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The Representation of Constraints by Means of an Electronic Differential Analyzer*

DONALD T. GREENWOOD†

Summary—The use of high gain amplifiers is shown to be helpful in the representation of constraints. This method enables one to represent constrained systems in a manner such that all coordinates are available for the application of arbitrary forces or displacements. The procedure is explained by means of an example.

Introduction

THE ANALYSIS of physical systems on analog computers quite frequently involves equations of constraint. These equations of constraint are usually of the form

$$f(q_1, q_2, \cdots, q_n) = 0 \tag{1}$$

where the q are coordinates.

A straightforward method of analyzing these systems is to use the equations of constraint to reduce the number coordinates that are used in the analysis so that only independent coordinates remain. This procedure is often appropriate. However, it suffers from a lack of flexibility in the analog setup because coordinates have been removed from the analysis and are no longer available for the direct application of forces or further constraints.

The method presented here enables one to apply the equations of constraint to the system and still have all the coordinates available. The practical advantage is that the analog representation of a system with constraints may be tested under a wide variety of conditions without having to change the basic computer setup.

Subsystem Equations

The procedure will be illustrated by means of an example. (See Fig. 1.) Each of the three subsystems can be analyzed in a straightforward manner if the constraining forces exerted by the rigid lever can be obtained.

The subsystem equations are

$$m_1\ddot{x}_1 + k_1x_1 = F_1 \tag{2}$$

$$b_2\dot{x}_2 + k_2x_2 = F_2 \tag{3}$$

$$m_4\ddot{x}_4 + b_4\dot{x}_4 = F_3 \tag{4}$$

$$k_3(x_3 - x_4) = F_3. \tag{5}$$

The computer representation of these equations is obtained by standard means[1] and is shown in Fig. 2.

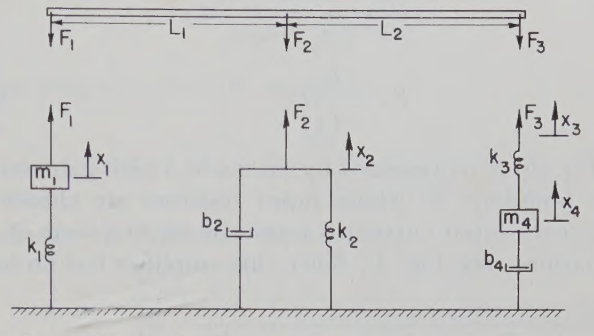


Fig. 1—The mechanical system broken into subsystems.

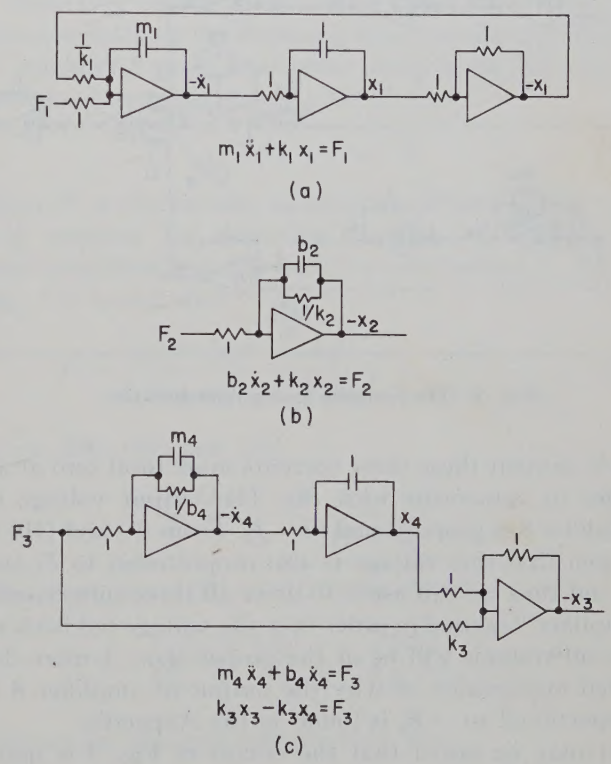


Fig. 2—The computer representations of the subsystems.

The Equation of Restraint

The equation of constraint imposed upon the coordinates by the rigid lever is expressed by

$$\frac{x_2 - x_1}{L_1} = \frac{x_3 - x_2}{L_2}$$

or

$$-L_2x_1 + (L_1 + L_2)x_2 - L_1x_3 = 0. \tag{6}$$

In addition, one can solve directly for the forces F_2 and

* Manuscript received by the PGEC, August 24, 1955; revised manuscript received May 21, 1956.

† University of Michigan, Ann Arbor, Michigan.

[1] G. A. Korn and T. M. Korn, "Electronic Analog Computers," McGraw Hill Book Co., Inc., New York, N. Y., pp. 22–53; 1952.

F_3 in terms of F_1. The equations of equilibrium of the lever are

$$F_1 + F_2 + F_3 = 0 \tag{7}$$

$$F_1 L_1 - F_3 L_2 = 0. \tag{8}$$

From (7) and (8) we obtain

$$F_2 = -\frac{L_1 + L_2}{L_2} F_1 \tag{9}$$

$$F_3 = \frac{L_1}{L_2} F_1. \tag{10}$$

Eq. (6) is represented by means of a high gain amplifier (amplifier 8) whose input resistors are chosen so that each input current is proportional to a term of the equation. (See Fig. 3.) Since this amplifier has no feedback element these three currents must total zero at all times in agreement with (6). The output voltage of amplifier 8 is proportional to $-F_1$. From (9) and (10) it is seen that this voltage is also proportional to F_2 and F_3 and thus we can use it to drive all three subsystems. Amplifier 9 is used in order that the voltage fed back to the subsystems will be of the proper sign. A more detailed explanation of why the output of amplifier 8 is proportional to $-F_1$ is found in the Appendix.

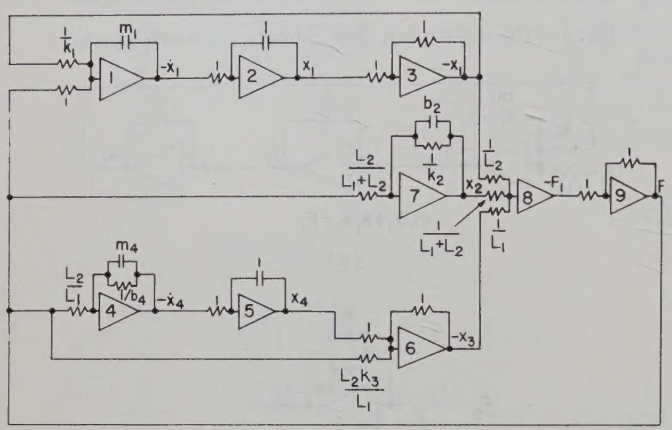


Fig. 3—The complete analog representation.

It may be noted that the circuit of Fig. 3 is quite flexible in that it may be driven at any coordinate or further constrained without changing the basic circuit. For example, force inputs at x_1, x_2, or x_4 are accomplished by using a driving voltage corresponding to the desired force at the inputs of amplifiers 1, 7, or 4, respectively. A force at x_3 is represented by inputs to amplifiers 4 and 6. A force between x_3 and x_4 is represented by an input to amplifier 6.

Suppose that the system is to be further constrained by

$$x_3 = 0. \tag{11}$$

This would be accomplished by removing the input to amplifier 8 from amplifier 6. For this case amplifiers 4, 5, and 6 can be put in a standby condition since x_3 and x_4 as well as their derivatives are zero. In a similar manner, x_1 or x_2 could be held fixed without changing the basic circuit.

In fact, the circuit of Fig. 3 can be used to analyze the response of the system when driven by an arbitrary force or displacement at any of the coordinates.

The Conventional Approach

Suppose that the mechanical system of Fig. 1 is represented in the conventional manner. Eq. (6), the equation of constraint, can be used to eliminate x_3.

$$x_3 = \frac{-L_2 x_1 + (L_1 + L_2) x_2}{L_1}. \tag{12}$$

Substituting (12) into (5), we obtain

$$-k_3 \frac{L_2}{L_1} x_1 + \frac{k_3(L_1 + L_2)}{L_1} x_2 - k_3 x_4 = F_3. \tag{13}$$

From (13) and (10) an expression for F_1 can be obtained.

$$F_1 = \frac{k_3 L_2}{L_1^2} [-L_2 x_1 + (L_1 + L_2) x_2 - L_1 x_4]. \tag{14}$$

The circuit representing (2), (3), (4), and (14) is shown in Fig. 4. Note that this circuit is the same as that of Fig. 3 except that amplifier 8 now has a feedback resistor and the input connection to amplifier 6 from amplifier 9 has been removed. Also, amplifier 10 has been added. The feedback resistor of amplifier 8, $L_2 k_3 / L_1^2$, provides a direct feedback path equivalent to that which existed in the circuit of Fig. 3 and which included input resistors $L_2 k_3 / L_1$ and $1/L_1$.

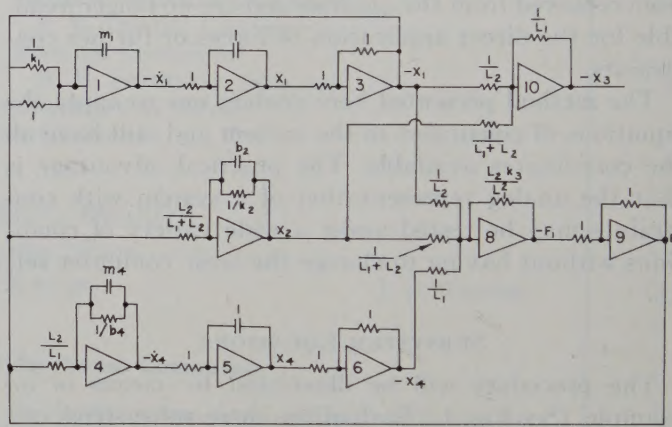


Fig. 4—The complete analog representation using conventional methods.

The conventional circuit of Fig. 4 is not as flexible in its use as the circuit of Fig. 3. For example, suppose one desires to drive the system with a prescribed displacement x_3. This cannot be done with the circuit of Fig. 4. However, using the circuit of Fig. 3, one immobilizes amplifiers 4, 5, and 6 and drives amplifier 8 through the input resistor $1/L_1$ with a voltage $-x_3$.

In case one desires to solve for the motion of x_4 due to a prescribed x_3, only the third subsystem is involved. Amplifiers 1, 2, 3, and 7 are immobilized and an additional input voltage x_3 is applied to amplifier 8 through an input resistor $1/L_1$.

Stability

In some cases it is necessary to use a small feedback capacitor with amplifier 8 in order to prevent high frequency oscillations. Usually the capacitor is no larger than 100 $\mu\mu$f. At the frequencies encountered in problem solutions, this capacitor will cause no appreciable error in the result.

From (6) it can be seen that the equation of constraint could be differentiated with respect to time, giving an equation in terms of velocities. One normally has fewer oscillation difficulties by using this form of the constraint equation, providing that these terms are available in the circuit. However, such a circuit will be more sensitive to amplifier drift errors.

Nonholonomic Constraints

Consider now the representation of nonholonomic constraints. In this case, the conventional approach cannot be used because the equation of constraint cannot be solved explicitly for one of the variables in terms of the others. The proposed method of representing constraints by means of high-gain amplifiers, however, is applicable in this case also. The terms of the equation of constraint are fed in as currents to the summing junction of the high-gain amplifier. These input terms normally contain time derivatives of the coordinates. In this case the output voltage of the high-gain amplifier corresponds to a force of constraint.

Other Constraining Equations

In some instances it is more convenient to express a constraint in terms of forces rather than displacements or velocities. In this case the analog computer representation would use a high-gain amplifier whose inputs correspond to forces. The output voltage would represent a coordinate or one of its time derivatives. As in the previous example, this circuit would exhibit considerable flexibility in its operation.

Appendix

In order to see more clearly that the output of the high-gain amplifier (amplifier 8 of Fig. 3) actually corresponds to $-F_1$, consider the representation of the mechanical system of Fig. 1 under the following conditions. Assume that the mechanical system is driven at x_1. The transfer function relating F_1 and x_1 is to be calculated. First write the equations of the individual subsystems.

$$F_1 = Y_1 x_1 \tag{15}$$

$$F_2 = Y_2 x_2 \tag{16}$$

$$F_3 = Y_3 x_3 \tag{17}$$

where Y_1, Y_2, and Y_3 are operators. From (2) and (3) we note

$$Y_1 = m_1 p^2 + k_1 \tag{18}$$

$$Y_2 = b_2 p + k_2. \tag{19}$$

From (4), (5), and (17)

$$Y_3 = \frac{k_3(m_4 p^2 + b_4 p)}{m_4 p^2 + b_4 p + k_3}. \tag{20}$$

From (16), (17), and (6) we obtain

$$-L_2 x_1 + (L_1 + L_2)\frac{F_2}{Y_2} - L_1 \frac{F_3}{Y_3} = 0. \tag{21}$$

From (9), (10) and (21) there results

$$x_1 = -\left[\left(\frac{L_1 + L_2}{L_2}\right)^2 \frac{1}{Y_2} + \left(\frac{L_1}{L_2}\right)^2 \frac{1}{Y_3}\right] F_1. \tag{22}$$

Returning now to the circuit of Fig. 3, the sum of the currents entering the summing junction (the grid node) of amplifier 8 must total zero. Designating the output voltage of amplifier 8 by e_8, we obtain

$$-x_1 L_2 + Y e_8 = 0 \tag{23}$$

where Y is the transfer admittance defined as the current entering the summing junction of amplifier 8 from amplifiers 6 and 7 due to a unit voltage e_8. From Fig. 3 it is seen that

$$Y = \frac{(L_1 + L_2)^2}{L_2(b_2 p + k_2)} + \frac{L_1^2}{L_2 k_3} + \frac{L_1^2}{L_2 p(m_4 p + b_4)}. \tag{24}$$

From (18), (19) and (24)

$$Y = \frac{(L_1 + L_2)^2}{L_2}\frac{1}{Y_2} + \frac{L_1^2}{L_2}\frac{1}{Y_3}. \tag{25}$$

Therefore, from (23) and (25) we obtain

$$x_1 = \left[\left(\frac{L_1 + L_2}{L_2}\right)^2 \frac{1}{Y_2} + \left(\frac{L_1}{L_2}\right)^2 \frac{1}{Y_3}\right] e_8. \tag{26}$$

Comparing (22) and (26) we note that

$$e_8 = -F_1. \tag{27}$$

Thus it is seen that, for this example, the output voltage of amplifier 8 corresponds to $-F_1$. A similar result would be obtained if the system were driven at a coordinate other than x_1.

Acknowledgment

In the past several years, during which time we have used the above method with increasing frequency, a number of people have contributed to its development. Among these are W. J. Davis and R. F. O'Connell, of Lockheed Aircraft Corporation and G. A. Korn. Their ideas have been most helpful.

High-Speed Shift Registers Using One Core Per Bit*

V. L. NEWHOUSE† AND N. S. PRYWES‡

Summary—A three, and a two winding per core, high-speed, current driven, one core per bit shift register is presented together with an analysis of the basic circuit involved. An intermediate storage capacitor is used between successive logical elements. The charge and discharge of this capacitor are controlled in a positive manner by voltage blocking pulses. The undesired feedback of energy from one stage to earlier stages is thereby prevented, giving high efficiency of operation. The three winding per core register described is reversible and capable of operating in the megacycle range. The application of the basic shift register element to computer logic applications is described.

Introduction

THE USE OF one core per bit registers for performing the logical operations in a computer has been under consideration for some time [1]. It is desired to present here the operation of a circuit of this type which has some special features to recommend it. The most important among these are:

1) Stable and nonmarginal operation which is independent of variations in the core material and in which the building-up of spurious pulses is blocked.
2) A very simple manner of operation which permits a straightforward and reliable design procedure.
3) A means of completely blocking the transfer of energy in a direction opposite to that of the information flow. This allows high-speed operation with comparatively low-power dissipation in the transfer loop.
4) The possibility of operating as a reversible shift register.

The disadvantages of this circuit in comparison with the previously suggested one [1], are in the required use of an additional diode and of a blocking pulse. It is felt, however, that the advantages exceed the disadvantages particularly for operation in the region above 100 kc.

Basic Circuit Operation

Consider, first, the operation of the basic shift register as shown in Fig. 1. Each element of the shift register consists of the following components: a square loop magnetic core with input, output, and advance windings, the characteristic of which is shown in Fig. 2(a); a capacitor C which provides intermediate energy storage; two diodes D_1 and D_2 which conduct during the charging and discharging of capacitor C, respectively; and a blocking pulse V_R which keeps the diode D_2 open-circuited during the period of charging the capacitor C. In addition, if it is so desired, a constant blocking voltage V_B may be used with the purpose of accelerating the reversal of flux in the case of "ones" and blocking the pulses which result from "zeros." This will be further discussed below.

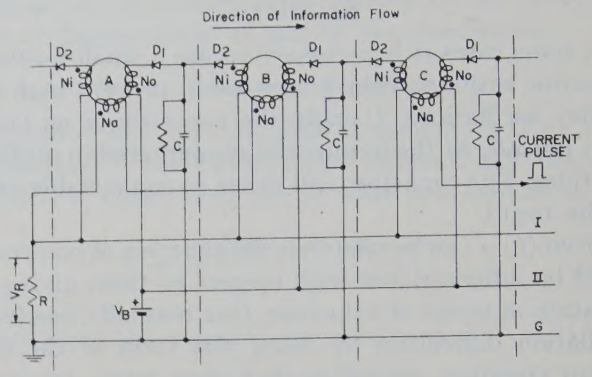


Fig. 1—Magnetic one core per bit, single line shift register.

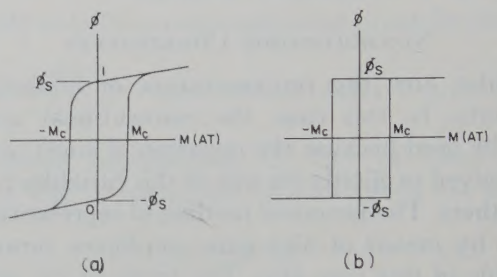


Fig. 2—(a) Flux—mmf characteristic of a magnetic core. (b) Idealized characteristic.

The operation of the circuit is as follows: positive remanent flux at saturation is associated with a "one" and negative remanent flux at saturation with a "zero." If core B of Fig. 1 stores a "one" and cores A and C store "zeros," then an advance pulse will move the "one" from core B to core C leaving a "zero" in core B. As the current advance pulse is applied, capacitor C is charged negatively through diode D_1. A blocking pulse V_R keeps diode D_2 open-circuited for the duration of the advance pulse. During the advance pulse, flux reversal occurs in core B. At the termination of the advance pulse, capacitor C is discharged through diode D_2 reversing the flux in core C.

With a zero stored in a core, the advance pulse will induce a negative voltage pulse in the winding. This pulse will be of a duration corresponding approximately to the rise time of the advance pulse and its amplitude will depend on the characteristic of the core at saturation and on the rise time of the advance pulse. A series of such pulses will build up the voltage across the capacitor to the peak amplitude of these pulses. This voltage may be further amplified in each stage of the register

* Manuscript received by the PGEC, October 6, 1955; revised manuscript received June 6, 1956.
† RCA, Camden, N. J.
‡ Sperry-Rand Corp., Philadelphia, Pa.

until finally a spurious "one" is inserted. It is desirable to block this phenomenon. In Fig. 1, this is achieved by biasing the output winding with a voltage V_B equal to the amplitude of the pulses induced in the case of "zeros." In this way, the diode D_1 is held open until the output voltage exceeds this value, which occurs only when storing a "one." The advantage of this scheme is that the blocking voltage also accelerates the reversal of flux. The disadvantage is that the noise cancellation is achieved at the expense of dissipating energy in the supply V_B. This has to be supplied by the advance pulse.

Another way of blocking the building-up of zeros is shown in Fig. 3. Here a bucking core identical to the

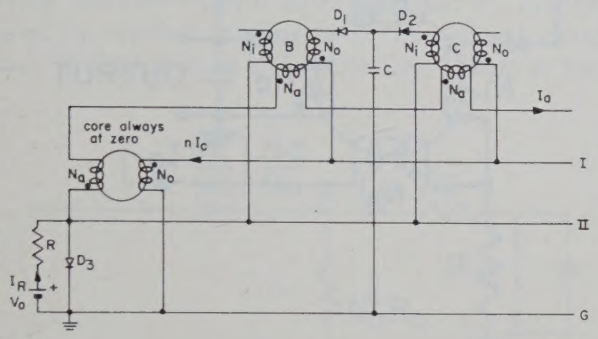


Fig. 3—Alternate method of blocking "zeros" from building-up and of generating a blocking pulse.

other cores but with advance and output windings only is used.[1] The bucking core is always at a state corresponding to a "zero." In the case of n "ones" stored in the shift register, the total effect is similar to that of applying to the bucking core a pulse approximately $(n+1)$ times greater than the advance pulse ampere turns. Thus the pulse induced in the output winding of the bucking core more than cancels the pulses generated by "zeros" in the respective stages of the shift register. The duration of the bucking pulse as well as that of the "zero" pulses corresponds approximately to the rise time of the advance pulse. This method has the disadvantage of delaying the beginning of the charging of the capacitors in stages containing "ones."

The function of blocking zeros can be achieved by other schemes of which the above are representative.

The transfer of a unit of information from one core to the next in the circuit of Fig. 1 is illustrated by the waveforms of Fig. 4.

The waveshapes are drawn one under the other in the proper time relationship. At the application of the advance pulse I_a shown at the top, voltage is induced in the output winding. Since no current flows until the bias voltage V_b is overcome, the output voltage changes by this much very rapidly. Following this, current flows in the charging loop and the voltage is determined by

[1] The feasibility of using a single bucking core to serve a multiple core register was suggested to the authors by R. E. Wilson.

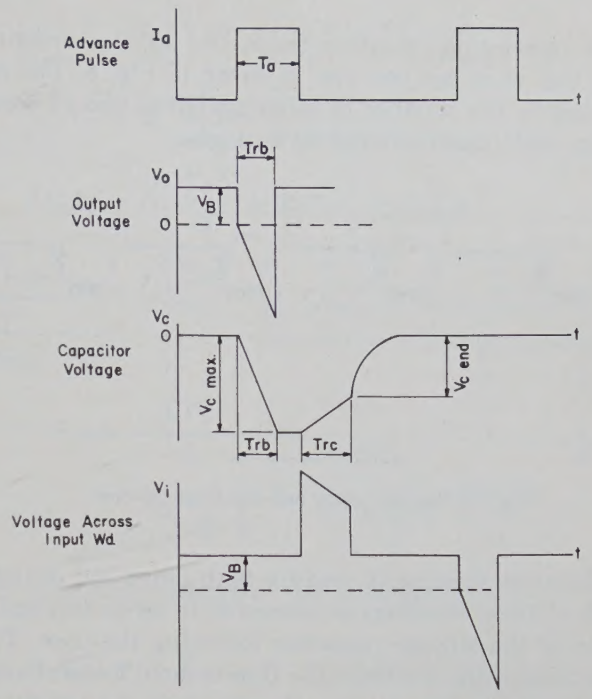


Fig. 4—Shift of "one" from core B to core C (Fig. 1). Initially, "zeros" are stored in cores A and C.

the charge developed at the capacitor. At the conclusion of flux switching, the output voltage returns rapidly to the bias voltage value.

The charging of the capacitor is nearly linear due to the nearly constant charging current. At the conclusion of charging time T_{rb} both diodes D_1 and D_2 become nonconducting, until the termination of the advance pulse. Then the capacitor discharges through the input winding of the succeeding stage and switches the flux in the respective core in the time T_{rc} storing a "one" in this core. The input voltage of the succeeding stage is shown on the lowest line of Fig. 4, showing also the voltage developed in the input winding when the "one" is read out of this stage by the next advance pulse.

Circuit Variations

The symmetry of the circuit of Fig. 1 suggests the possibility of operating the shift register in a reversible manner. Reversal of information flow in a register of the type of Figs. 1 or 3 has been demonstrated and is accompanied by a reversal of the direction of charge of the intermediate storage capacitors. It is necessary to interchange the two types of bias applied to lines I and II. At the same time the polarities of the bias voltages must be inverted, *i.e.*, in Fig. 1 a negative bias V_B is applied to line I and a positive going blocking pulse to line II. As it is not easy to achieve polarity reversal of the blocking pulse using the resistor circuit shown in Figs. 1 and 3, some more elaborate technique of blocking involving a pulse transformer is required. When information progresses from right to left in a register of the type of Fig. 1, the capacitors are charged positively rather than negatively.

An interesting modification of the register utilizing only two windings per core is shown in Fig. 5. The reduction in the number of windings gives rise to some design and constructional advantages.

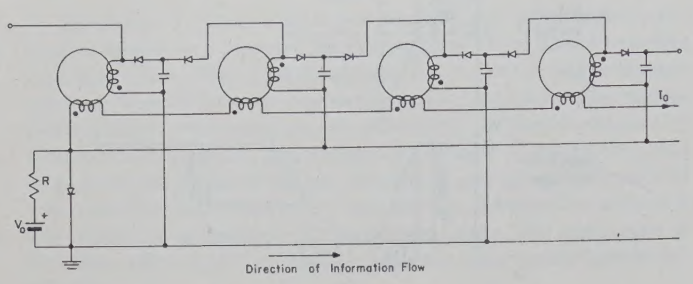


Fig. 5—Register using two windings per core.

The same winding is used for both input and output. Each of these windings is connected in series through a diode to the storage capacitor following the core. The directions of the diodes in the thus created loops change alternately so that the capacitors can charge positively and negatively in alternate stages. In Fig. 5, starting from the left, the odd capacitors can be charged only negatively and the even capacitors can be charged only positively.

The loops created by the output windings and the capacitors are grounded in the odd stages and are pulsed negatively in the even stages by pulses which last for the duration of the advance pulses I_a. The effect of these pulses is to bias in the reverse direction the diodes between all loops, rendering them nonconducting for the duration of the advance pulses. The advance pulses then induce a voltage to charge the capacitors following the cores storing "one," without interference of one stage with another. At the conclusion of the drive pulses, the capacitors discharge through the windings of the successive stages, storing "one" in them. For simplicity, the bias voltages blocking the build-up of zeros have not been shown in Fig. 5. Such negative and positive voltages would be inserted in the loops of the odd and even stages respectively.

The unit element of the step register circuit of Fig. 1 can be regarded as a member of the class of half-cycle response magnetic amplifiers. One element can be used to feed many others. Digital logic circuits can be built up by replacing the capacitor charging diode by conventional OR-AND-OR resistor diode networks.

Operation as a bistable memory device is illustrated in Fig. 6. Here the output is connected to the input winding of the same stage. Thus, information read out of the core is temporarily stored in the output capacitor and then regenerated into the core itself. A set pulse will cause the initial storing of a "one" which will be regenerated until a reset pulse is introduced which cancels the regeneration during one cycle, following which no output will appear. Thus, the bistable element of Fig. 6 constitutes a dynamic flip-flop.

Analysis of the Basic Circuit Operation

The operating cycle can be divided into two distinct parts associated with the charge and discharge of the intermediate storage capacitor. Making suitable assumptions, each phase of the operation can be represented by a set of linear differential equations. By integrating these and matching the boundary conditions, a complete solution is readily obtained.

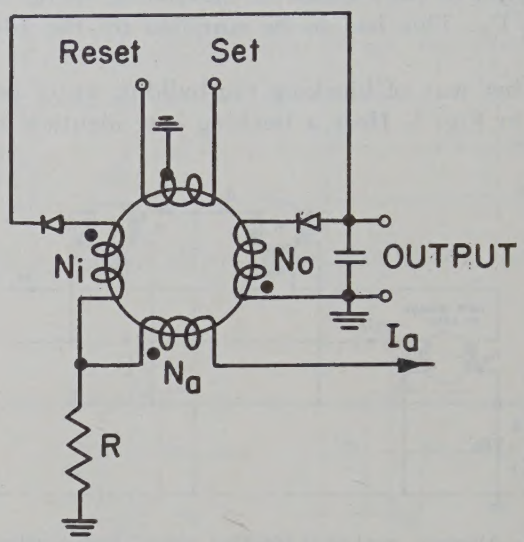
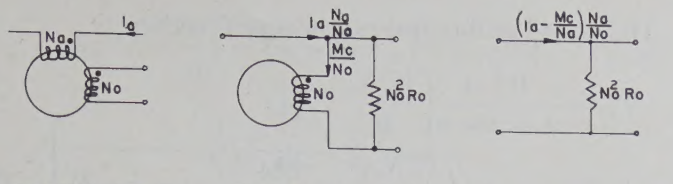


Fig. 6—A bistable element.

The operation of the core, on passing through a major hysteresis loop, justifies approximating its characteristic by the square loop of Fig. 2(b) and accounting for eddy current and relaxation losses by introducing an equivalent resistance in shunt with the winding. This concept of equivalent resistance corresponds with previous work [3, 4]. In this manner current losses as well as energy losses are accounted for. These losses are proportional to the change in flux. The equivalent resistance representing these losses will be proportional to the square of the number of turns of the winding across which it is shunted. The resistance per turn will be referred to as R_0. A method for the experimental determination of this equivalent resistance is described below.

The method of deriving equivalent circuits for the core windings during flux reversal is shown in Fig. 7. Since the currents through the windings during flux reversal are approximately constant, we can define the forward resistance of the diodes, R_f, as the ratio of the voltage drop across the diode to the current. The back resistance of the diodes is assumed to be infinite. The resistances across the Fig. 1 capacitors are intended to prevent the capacitors from charging to V_B in the absence of advance pulses. These resistances are of a magnitude of several thousand ohms and are small in comparison with the back resistance of the diodes. Their effect on the pulse operation can be neglected. The circuit operation will be determined, acting on the simplifying assumptions detailed above.



(a) THE ACTUAL CIRCUIT (b) EQUIVALENT CIRCUIT UNDER SIMPLIFYING CONDITIONS DURING REVERSAL OF FLUX. (c) EQUIVALENT CIRCUIT FURTHER SIMPLIFIED.

Fig. 7—Equivalent circuits according to simplifying assumptions.

Charging Cycle

During the charging of the intermediate storage capacitors, diodes D_2 are held open-circuited by the pulse V_R and current flows only in the output windings. Let the advance current be of duration T_a, amplitude I_a and be applied at time $t=0$. The actual charging circuit is simplified to the equivalent circuit of Fig. 8.

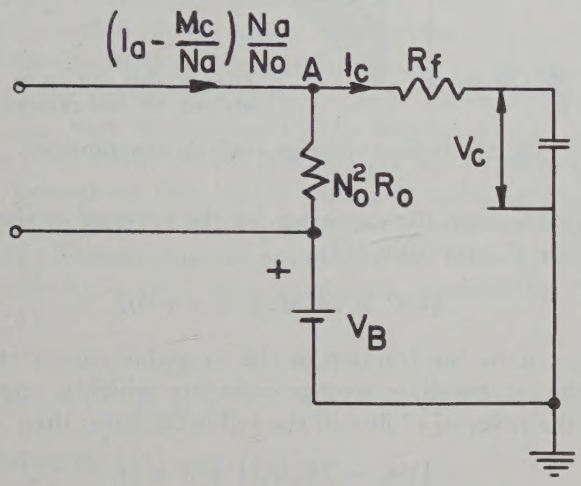


Fig. 8—Simplified equivalent charging circuit.

The solution of the nodal equation at point A (Fig. 8) for the period of flux reversal T_{rB}, of the charging core gives the expression for the charging current I_C. This expression, when integrated, gives the voltage across the corresponding capacitor. A further integration of the voltage equation of the loop of Fig. 8 gives the total change of flux in the core, equal to $2\Phi_S$. These equations can be simplified by replacing all exponential terms by the first and second order terms of their respective series expansion. This is justifiable provided that the flux reversal time T_{rB} is much shorter than the time constant of the circuit.

$$T_{rB} < C(R_0N_0^2 + R_f). \tag{1}$$

If, in addition, the condition

$$R_0N_0^2 \gg R_f \tag{2}$$

is fulfilled, further simplification is possible and the equations for the charging cycle become:

$$\begin{aligned} I_c &= I_0\left[1 - \frac{t}{CR_0N_0^2} + \frac{1}{2}\left(\frac{t}{CR_0N_0^2}\right)^2\right] \\ V_c &= I_0\frac{1}{C}\left[t - \frac{1}{2}\frac{t^2}{CR_0N_0^2}\right] \\ 2N_0\Phi_s &= I_0\left[\frac{T_{rB}^2}{2C} + R_fT_{rB}\right] + V_BT_{rB} \\ I_0 &= I_a\frac{N_a}{N_0} - \frac{M_c}{N_0} - \frac{V_B}{R_0N_0^2}. \end{aligned} \tag{3}$$

Then:

$$\begin{aligned} T_{rB} = &-\frac{CV_B}{I_0} - CR_f \\ &+ \sqrt{\left(\frac{CV_B}{I_0} + CR_f\right)^2 + \frac{4CN_0\Phi_s}{I_0}}. \end{aligned} \tag{4}$$

The maximum voltage of the capacitor will be

$$V_c(t = T_{rB}) = -V_{c,\max} = -\frac{I_0}{C}\left(T_{rB} - \frac{T_{rB}^2}{2CR_0N_0^2}\right). \tag{5}$$

Conditions (1) and (2) should be satisfied in the design to minimize losses. Hence, (3), (4), and (5) can be used for all practical design purposes.

The considerations determining the amplitude of the pulse V_R blocking the diodes D_2 for the duration of the advance pulse are as follows: V_R should be larger than the sum of $V_{c,\max}$ and the voltage induced in the input winding of the following core, when both that core and the preceding one are undergoing a major flux change. This requirement is satisfied by the condition

$$V_R = I_aR > V_{c,\max}\left(1 + \frac{N_i}{N_0}\right). \tag{6}$$

It is clear that to insure complete flux reversal and to prevent premature discharge of the intermediate storage capacitor, the duration of the advance pulse, T_a must be kept greater than the time of flux reversal in the driven core T_{rB}.

Discharging Cycle

The discharge of the intermediate storage capacitor through the diode D_2 and the input winding of the core of the next stage, starts at the time of the termination of the advance pulse which will now be indicated by $t=0$.

The equivalent simplified discharge circuits for n stages are shown in Figs. 9 and 10. Expressions for the capacitor discharge current I_d and voltage V_c, during the flux reversal time T_{rC}, are again obtained by simple integration of loop and nodal equations. The flux reversal time T_{rC} is taken as short in comparison with the time constant of the loop of Fig. 10, *i.e.*,

$$T_{rC} < CN_i^2R_0. \tag{7}$$

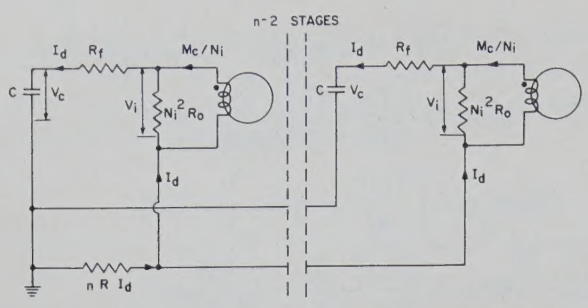


Fig. 9—Simplified equivalent discharge circuit of n stages.

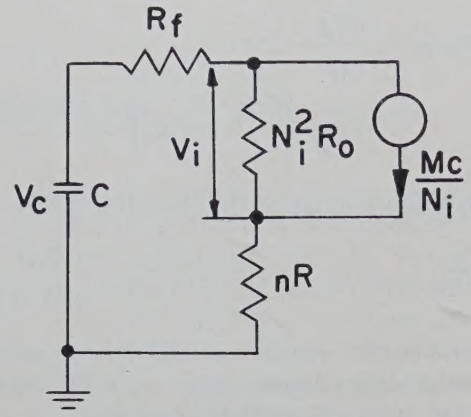


Fig. 10—Simplified equivalent discharge circuit.

This enables the exponential terms to be replaced as above by the first and second terms of their series expansion. In this process

$$V_{c,\max} - V_{c,\text{end}} = \frac{1}{C}\int_0^{T_{rC}} I_d dt = N_i \frac{1}{C}\left[M_c T_{rC} + \frac{2\Phi_s}{R_0}\right]. \quad (8)$$

Eq. (8) shows a way to measure R_0 independently of the voltage drops across diodes and resistances. $V_{c,\max}$ and $V_{c,\text{end}}$ are the voltages across the capacitor at the beginning and end of flux reversal. These, as well as T_{rC}, are simple to distinguish on inspection of voltage waveforms occurring across the capacitor. Eq. (8) therefore, indicates a convenient means of obtaining R_0 experimentally under actual circuit operating conditions. Let

$$V = V_{c,\max} - \frac{M}{N_i}(nR + R_f). \quad (9)$$

$$a = \frac{nR + R_f}{R_0 N_i^2} \qquad b = \frac{V}{M_c N_i R_0}. \quad (10)$$

Using the notation and the simplifying assumptions stated above, the voltage across the input winding becomes

$$V_i = \frac{V}{1+a} - \frac{1+a+b}{(1+a)^2}\frac{M_c t}{CN_i}. \quad (11)$$

The period of flux reversal in core C is then:

$$T_{rC} = \frac{1+a}{1+a+b}\left[\frac{VCN_i}{M_c} - \sqrt{\left(\frac{VCN_i}{M_c}\right)^2 - \frac{4\Phi_s CN_i^2}{M_c}(1+a+b)}\right]. \quad (12)$$

As shown in Fig. 11, $V^2C/2$ is the maximum energy

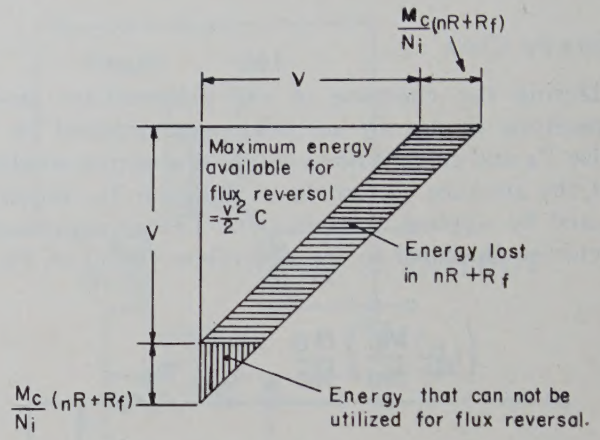


Fig. 11—Balance of energy available from capacitor.

available from the capacitor for the reversal of the flux in core C, and from (12)

$$\tfrac{1}{2}V^2C \geqq 2\Phi_s M_c(1+a+b). \quad (13)$$

Let K be the fraction of the available energy stored in the intermediate storage capacitor which is required for the reversal of flux in the following core; then

$$K\tfrac{1}{2}V^2C = 2\Phi_s M_c(1+a+b). \quad (14)$$

Then (12) can be written in the form

$$T_{rC} = \frac{1+a}{1+a+b}\frac{VCN_i}{M_c}(1 - \sqrt{1-K}). \quad (15)$$

Eqs. (11), (12), and (13) will be used in discussing the design of a register. At the termination of the flux reversal, the capacitor will discharge rapidly through the resistor R. This resistance should be made large enough to limit the current through diode D_2 to a safe value.

Additional Methods for Generating Blocking Pulses

The auxiliary task of generating a blocking pulse to keep diode D_2 open for the duration of the advance pulse can be accomplished in several ways. One way of performing this function is shown in Fig. 1. The condition (6) $V_r = I_a R$ may impose a large resistance R which will slow the discharge of the capacitor and the reversal of the flux. An alternate method is suggested in Fig. 3. In this case condition (6) is replaced by:

$$R\left(I_a - \frac{V_0}{R}\right) = V_R > V_{c,\max}\left(1 + \frac{N_i}{N_0}\right) \qquad (16)$$

$$I_a > \frac{V_0}{R} > nI_d.$$

The impedance of the blocking circuit in Fig. 3 to capacitor discharge is the forward impedance of D_3.

The discharge current is limited by inserting resistors in series with the discharge diodes. These resistances can be included in the value of R_f that corresponds to the forward resistance of the diode D_2. Further, in order to make (7) to (15) applicable to the blocking method of Fig. 3 the value of R should be reduced to that of the forward resistance of the diode D_3.

Some Design Considerations

In designing a stage of the shift register, the required duration of a cycle in which a "one" is shifted from one stage to the next is usually given. Hence, it is possible to choose the periods of flux reversal T_{rB} and T_{rC} and the duration of the advance pulse T_a which constitute the period of a cycle. In some cases, the value of $V_{c,\max}$ may be imposed by the output circuit.

Eq. (14) shows that b is indicative of the losses during reversal of flux. (a is generally quite negligible compared to b.) The change of energy in the core is $2\Phi_s M_{c_0}$; b times this will be lost in R_0. It is naturally desirable to keep b at a minimum. From (10), (14) and (15)

$$b = \frac{4\Phi_s}{T_{rC} M_c R_0} \frac{1 - \sqrt{1 - K}}{K} (1+a). \qquad (17)$$

As indicated ([3] and [4]),

$$S = \frac{2\Phi_s}{R_0} \qquad (18)$$

where S is defined as the product of the ampere turns of the drive current applied to a particular core and the corresponding flux reversal time of that core. Hence,

$$b = \frac{2S}{T_{rC} M_c} \frac{1 - \sqrt{1 - K}}{K} (1 + a). \qquad (19)$$

Since S/M_c is dependent on the core material only, b is independent of the size of the core. For $\frac{1}{8}$ mil thick, 4-79 Mo-Permalloy tape cores, $S/M_c \approx 3 \times 10^{-6}$ sec. Hence,

$$b = \frac{1}{T_{rC}} 0.6.\ 10^{-6} \frac{1 - \sqrt{1 - K}}{K}. \qquad (20)$$

Eq. (14) emphasizes the need to reduce the area and diameter of the magnetic core if low energy operation is to be attained, since Φ_s and M_c are proportional to the cross section and diameter of the magnetic material respectively. In practice the reduction in core diameter is limited by practical winding techniques.

For a given size of core the design considerations are as follows: initially, a value of K is chosen between zero and unity and a is taken as zero. Minimum loss of energy is achieved by using $K = 1$ but K may be taken as smaller in order to accelerate the reversal of the core and to assure complete flux reversal. C may now be obtained from (14) and N_i from (10) provided that a value for V is postulated. For an initial approach to a design, V may be taken as equal to $V_{c,\max}$. [Their exact relationship is given in (9).] The value of the input voltage just before the termination of flux reversal is:

$$V_{c,\text{end}} = \frac{V}{1 + a} \sqrt{1 - K}. \qquad (21)$$

Since a is taken initially as equal to zero it is possible to determine $V_{c,\text{end}}$ as well as the value of r, the resistor used to limit the current through the discharge diode D_2. This in turn determines the time of the discharge after flux reversal has taken place in the receiving core.

T_{rB} being given, it is now possible to obtain I_0 and N_0 from (4) and (5) if a value for the blocking voltage V_b is assumed. Alternatively, values for I_a, N_a, N_0 and V_b can be obtained from (4), (5) using the value of the "zero" blocking voltage V_b:

$$V_B = \frac{N_0}{N_a} \frac{\mu I_a N_0}{T_r}. \qquad (22)$$

T_r stands for the rise time of the advance pulse. μ represents the rate of change of flux with ampere turns at remanence.

The previously obtained value for r, should be included in the term R_f, in (4). Care should again be exercised not to exceed the permissible current through D_1 or the permissible back voltage across D_2.

Second order corrections are made by repeating the above calculations, substituting the initially obtained values of the parameters for a and $V - V_{c,\max}$ and correcting T_{rC} by the time required for the capacitor to discharge completely after flux reversal has taken place in the receiving core.

Experimental Results

Some voltage waveforms illustrating the transfer of a "one" followed by a "zero" through a three-unit register designed for a 6-microsecond operating cycle are shown in Fig. 12. These should be compared with the corresponding idealized waveforms in Fig. 4. It is noteworthy that the points where the circuit operation changes from one mode to the other are clearly distinguishable. The voltage spikes produced by the cores during the rise and fall periods of the advance pulses are explained by the finite core material permeability at remanence. This also accounts for the slight but definite "overshoot" of the capacitor voltage after the completion of the discharge. The transmission of the negative-going spikes produced by the output wind-

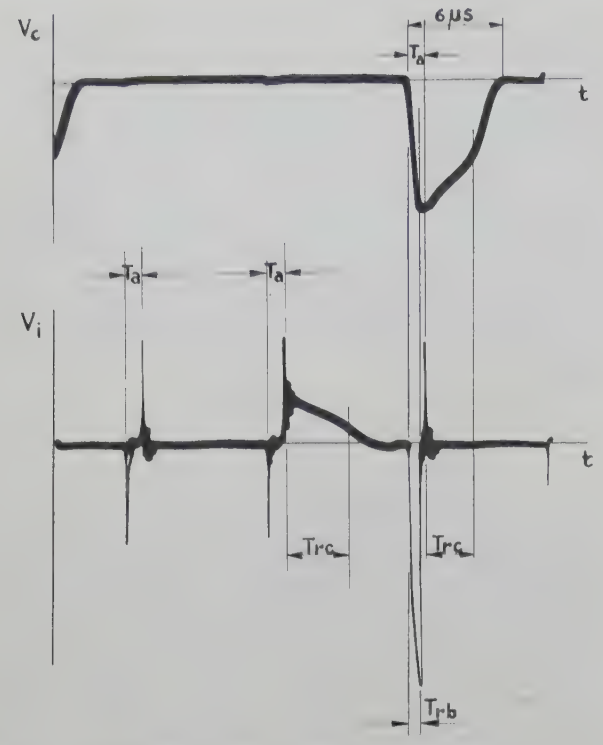


Fig. 12—Voltage wave shapes across output winding and the delay capacitator following a core, with 001 circulating in a three-core ring counter.

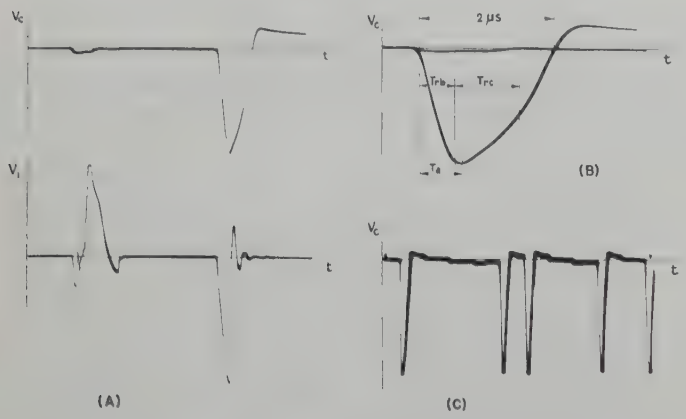


Fig. 13—(a) Voltage wave shapes across output winding and the delay capacitor following a core in the ten-core ring counter. (b) Comparison of "zero" and "one" voltages across the delay capacitor in the ten-core ring counter. (c) 1000110010 circulating in the ring counter.

ing is completely blocked by the bias voltage V_B.

The waveforms taken from a ten-unit register operating in a 2-microsecond cycle are shown in Fig. 13.

Both these registers utilized bobbins wound with $\frac{1}{8}$ mil thick Molybdenum Permalloy tape cores. The agreement between the calculated and measured waveform magnitudes was very satisfactory. Similar agreement has been obtained in the case of a two winding per core register of the type shown in Fig. 6.

Conclusion

The experimental results indicate that the circuits presented above lend themselves readily to analysis and are correspondingly easy to design. The use of blocking voltages results in economical operation and makes it possible to compensate for core imperfections in a straightforward manner.

List of Symbols

a = as defined by (10).
b = as defined by (10), (17), or (19).
C = storage capacitance.
K = portion of capacitor stored energy used for flux reversal.
I_a = advance pulse current.
I_c = charging current.
I_d = discharging current.
I_0 = as defined by (3).
M = mmf in ampere turns.
M_c = mmf in ampere turns corresponding to coercive field.
N_a = number of turns of advance winding.
N_i = number of turns of input winding.
N_o = number of turns of output winding.
n = number of cores in the shift register storing a one at the same time.
R = resistance of the blocking pulse source.
R_f = equivalent forward resistance of a diode.
R_0 = equivalent resistance of core for a single turn winding.
r = current limiting resistance to protect discharge diode.
T_a = duration of advance pulse.
T_r = rise time of advance pulse.
T_{rB} = flux reversal time of output core B.
T_{rC} = flux reversal time of input core C.
t = time.
V = as defined by (9).
V_b = bias voltage.
V_c = capacitor voltage.
$V_{c,\max}$ = maximum capacitor voltage.
$V_{c,\text{end}}$ = capacitor voltage at end of flux reversal.
V_i = input winding voltage.
V_r = amplitude of blocking pulse.
Φ_s = remanece flux at saturation.
μ = inductance per turn at saturation.

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High-Speed Flip-Flops for the Millimicrosecond Region*

Z. BAY† AND N. T. GRISAMORE‡

Summary—The problem of designing high-speed flip-flops has been approached by dividing the circuit operation into steady-state and switching functions, the steady-state function being assigned to a slave flip-flop and the switching function to a driving circuit. Circuits, using conventional components and having a resolving time of 10 mμsec, are described. Resolving times as low as 2 mμsec have been attained by using a special beam-deflection tube as the slave flip-flop. These circuits dissipate considerably less power in the intervals between switching than conventional circuits.

Introduction

THE SPEED of operation of conventional flip-flop circuits is ultimately limited by the maximum current rating of the tubes in the circuit. The current used to charge or discharge the circuit capacitances during a change of state must be supplied by the tubes that maintain the stable states. Such flip-flop circuits, therefore, if they are to be operated at high frequencies (>1 mc), should be designed so that the current in the conducting or "on" tube approaches the maximum current rating, subject to the power dissipation limits of the tube.

Basing a calculation on the above-stated consideration, the minimum switching time, t, will be roughly of the order of CV_f/I, where I is the current in the "on" tube and V_f is the voltage change which appears across the circuit capacitance C when the flip-flop changes state. As an example, take a 6J6 which has a low input and output capacitance. The maximum current rating is 15 ma and if V_f is 15 volts then t is about one mμsec per $\mu\mu$f. The capacitance C can be assumed to be at least 10 $\mu\mu$f so that t would be $\sim$10 mμsec for this case. This is rough lower limit for t. For actual circuits its value would be considerably larger, primarily because all of the circuit capacitances are not charged or discharged simultaneously with the peak current I.

Another fact to be considered in the design of flip-flop circuits is that, although a 50 per cent duty cycle would be the most efficient operation, still the tubes might have long "on" periods. The usual design, therefore, is based on conditions that can occur during such a long "on" period. The development of circuits which operate with shorter switching times than mentioned above and whose standby ("on" period) power consumption is only a small part of the power consumption occurring during switching will be shown in this paper.

It should be noted that this paper represents a study of a method of switching and as such does not include the effects of tolerances or variation of the characteristics of circuit components with time. The circuits shown in Figs. 2 and 5 have all been constructed and operated, but only for the purpose of demonstrating the ideas of this paper.

Slave Flip-Flops

The tubes of a conventional flip-flop circuit have two functions: to provide power for rapid switching and to maintain the steady states. The former of these functions requires a considerably larger amount of power than is required by the latter. If, therefore, the power for switching is provided by an external source, then the standby power, required only to hold the steady states, can be reduced considerably. Such a flip-flop will be called a slave flip-flop in this paper. The use of a slave flip-flop allows one to design the complete flip-flop circuit (slave flip-flop plus driving circuit) without being limited by high-power consumption during long "on" periods. These two functions, as they apply to slave flip-flops, will now be described separately.

Switching is accomplished by supplying charge from an external source to the various circuit capacitances that change voltage. The time t required to charge or discharge these capacitances C can be obtained from the relation

$$\int_0^t I\,dt = CV_f,$$

where V_f is the voltage change and I is now current supplied by the *external* source. If I is constant or denotes the average value of the current over the time t, then

$$t = CV_f/I. \tag{1}$$

From (1) it is obvious that, for high-speed operation, C and V_f should be as small as possible while I should be as large as possible. The magnitude of I, which is somewhat dependent on V_f, is discussed under the section on "Complete Flip-Flop Circuits."

Storage is accomplished by either or both of two effects: 1) the charge delivered to C will be preserved for a time determined by RC where R is the resistance shunting C, and 2) the potential of C is kept constant

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by the tube current corresponding to the steady states. The first is responsible for short time memories after switching while the second holds the memory for any long period. It is an important feature of the slave flip-flop that even if, after switching, some time delays occur in operation 2), the memory is maintained by 1) if RC sufficiently overlaps the delays of 2), *e.g.*, transit time effects in the flip-flop tubes can be compensated for by a sufficiently large RC.

The driving circuit, consisting of two tubes, operates only during a change of state. One of these tubes drives the slave flip-flop into one state and the other into the opposite state. Therefore, the peak power output of the driving tubes can be at least twice the allowable power dissipation since the driving tubes operate with only a 50 per cent duty cycle. This means that the operating speed can be at least twice as great using slave flip-flops when compared with conventional arrangements. An even higher operating speed can be achieved for short periods, *e.g.*, the counting of pulse groups or pulses randomly spaced in time.

Without loss in generality, a driven slave flip-flop (Fig. 1) could be represented as having only two points

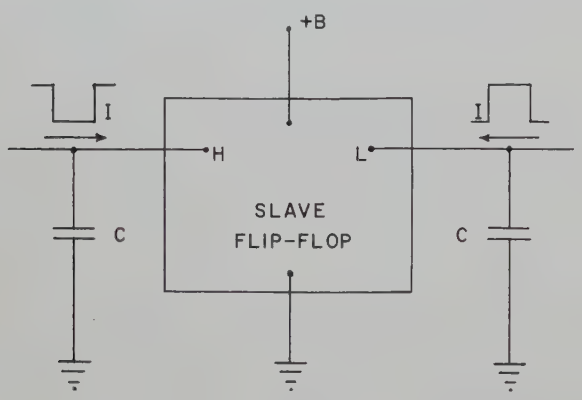

Fig. 1—Method of driving a slave flip-flop.

(H and L) which change voltage for a change of state of the circuit. In the particular situation illustrated, the voltage at H is greater than at L, and the current pulses must be of a magnitude and polarity such that the state will be changed. Of course, these pulses must be large enough to invert the state completely since the flip-flop is assumed to contribute nothing to the change of state process. The polarity of the pulses must alternate for each change of state. Methods for producing this alternation are discussed later.

In principle, any conventional flip-flop circuit can be operated as a slave flip-flop. Our choice, however, is directed towards flip-flops having only two voltage changes of equal amplitude but opposite phase such as Regener's circuit[1] and having a small voltage change [V_f small in (1) for high-speed operation]. A typical circuit of this type is shown in Fig. 2(a). Circuits of this type with a small V_f, although quite possible, are not very practical, since difficulties are encountered because of the variation in characteristics from one tube to another. (Circuits known at present having only one voltage change require large tube currents in the "on" position.[2] Recent developments in beam-deflection tubes seem to provide possibilities for the design and slave operation of flip-flops having only one voltage change.)

A circuit having only two voltage changes can be devised by using batteries as the voltage-dropping elements between the plate of one tube and the grid of the other tube. Thus, although the dc levels of the plate and grid are different, the change of voltage between the stable states is the same. Fig. 2(b) shows two circuits of this battery type, one using triodes and the other pentodes. The supply voltages for these battery circuits are lower than normal (15 to 60 volts) to enable the use of small batteries. Mercury cells were used because of their high ratio of battery capacity (amp-hr) to physical size. The particular cells that were used had a capacity of 80 ma-hr and ranged in voltage from 1.35 to 60.75 volts. The grids of the tubes are not operated at positive bias so grid current is small and presumably the batteries will last for an appreciable portion of the tube life. A voltage change of 4.5 volts was obtained with the triode circuit; even smaller changes (1.5 volts) were obtained with the pentode circuit. Matching of the two tubes is essential for such small changes of voltage. The battery circuit is very simple to design since only the cutoff voltage as a function of the plate voltage needs to be known.

To avoid using batteries, VR tubes can be used since the only essential feature of battery operation is the constant voltage drop. The circuit shown in Fig. 2(c) having a V_f of 10 volts illustrates this type of circuit. Although this particular circuit consumes 1.6 watts of power (about ten times the power of some of the battery circuits) this is still less than is usually associated with high-speed flip-flop circuits using vacuum tubes. There is no reason to believe that circuits of this type having a lower V_f and a lower power dissipation could not be designed.

Recently the National Union Electric Corp. developed a bistable memory element which operates as a beam deflection tube.[3] The beam can be held in either of two stable positions provided the proper plate resistors and supply voltages are used. Fig. 3 shows a diagram

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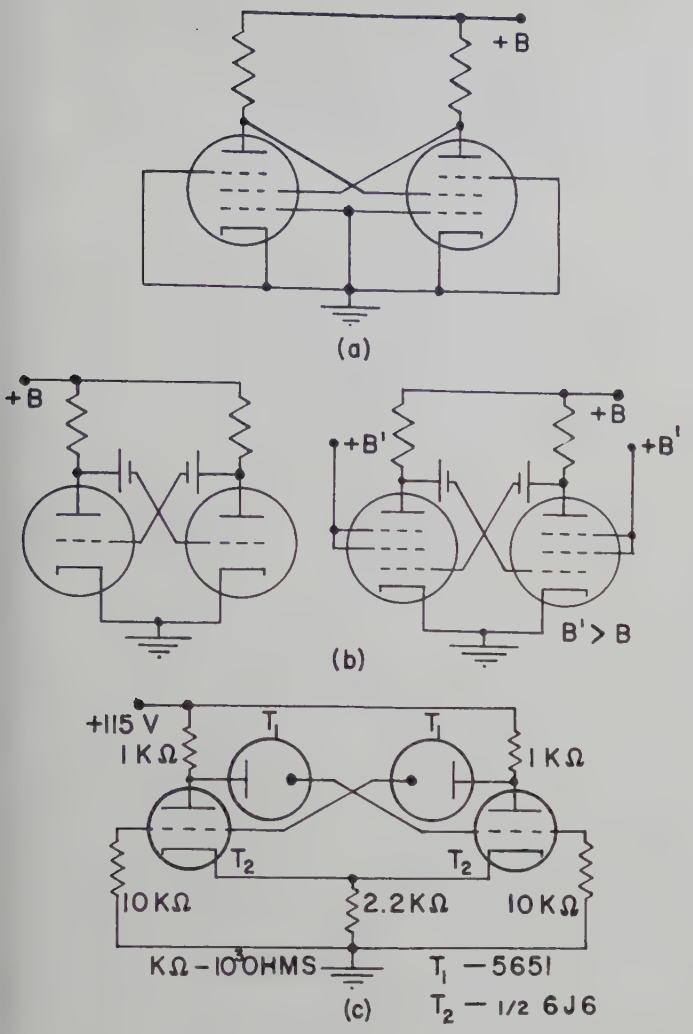

Fig. 2—(a) Direct-coupled pentode flip-flop. (b) Battery flip-flops. (c) VR-tube flip-flop.

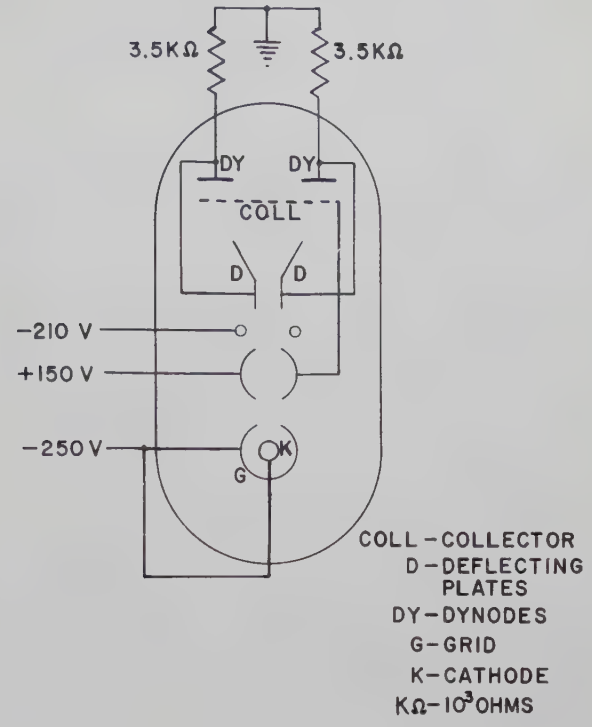

Fig. 3—Beam deflection tube as a bistable memory element.

of the tube and bistable circuit used as a slave flip-flop with a V_f of 7 volts.

Complete Flip-Flop Circuits

The combination of a slave flip-flop and a driving circuit is a complete flip-flop circuit. The driving circuit should operate from repeated signals of one polarity and should produce driving pulses of alternating polarity since the flip-flop must be driven in the opposite direction for each successive change of state. In order to achieve high-speed operation the peak current of the driving pulses should be as high as possible.

The most apparent method of producing driving pulses of alternating polarity from the input signals is to use two identical driving tubes, one being controlled by point H and the other by point L in Fig. 1. The requirements set for these driving tubes are as follows:

1) There should be no dc currents through the tubes during the steady states. Beside the fact that dc currents mean an unnecessary power dissipation, a bias above cutoff results in current pulses from both driving tubes during switching, only the difference of these pulses being effective for switching. A more serious objection is the need to reverse the steady-state condition resulting from the current through the driving tubes, *after* switching. Because of coupling between the driving and flip-flop tubes, part of the power necessary for this change must come from the slave flip-flop, in contradiction to slave operation. Thus, the bias of both driving tubes (determined by H and L in Fig. 1) should be below cutoff, the higher bias being preferably just at cutoff. (Cutoff, in this case, is the point at which the driving tube current is only a small fraction of that of the "on" flip-flop tube.) The difference between the biases is equal to the voltage V_f. To prevent a current output from both driving tubes, the input signal V_d (assumed to be a square pulse) should not be greater than V_f.

2) For high-speed operation the driving tubes should have high transconductance, sharp cutoff, small grid-base, and small input and output capacitance. Since the current I from the driving tubes is equal to $\bar{g}_m V_d$ where $\bar{g}_m$ is the current at the point V_d volts above cutoff divided by V_d, (1) can be written as

$$t = CV_f/\bar{g}_m V_d. \tag{2}$$

In the previous section it was shown that V_f can be reduced to quite low values. The best use of (2), therefore, results from using the highest $\bar{g}_m$ and the corresponding value of V_d. Having found V_d from the tube characteristics, V_f is set equal to V_d so that

$$t = C/(\bar{g}_m)_{\max}. \tag{3}$$

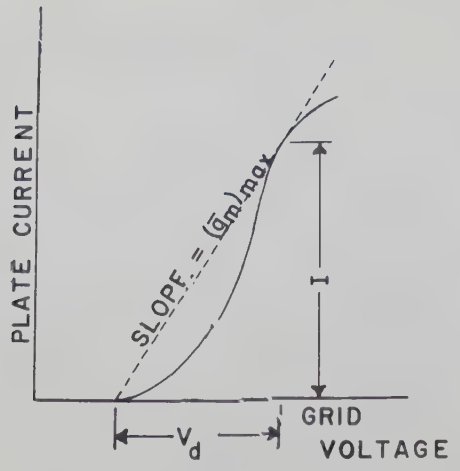

Fig. 4—Method used to find $(\bar{g}_m)_{max}$.

Fig. 4 shows the method used to find $(\bar{g}_m)_{max}$ and V_d from the transfer characteristics of the tube. Since the driving pulses, instead of being square shaped, have a finite rise time and the load includes resistance and inductance, the actual value of t is larger than that calculated from (3).

Experimental Circuits

The slave flip-flop circuits of Figs. 2(b), 2(c), and 3 have all been driven with EFP-60 tubes. Complete flip-flop circuits using these slave flip-flops are shown in Figs. 5(a), 5(b), and 5(c). Circuits have been constructed using triodes as phase inverters to provide the driving pulses but the fastest switching has been obtained by using EFP-60 secondary emission tubes as the source of driving pulses. The $(\bar{g}_m)_{max}$ for this tube is quite large (~20 ma/v) and if C is kept down to 30 $\mu\mu$f or less, then t should be of the order of 1 or 2 mμsec which is about the transit time in this tube. A memory of the previous state is provided by this transit time plus time delays occurring between the output of the EFP-60 and parts of the slave flip-flop. This essentially means that for trigger pulses of a few mμsec duration there will be little or no interference between the trigger pulse and the change of voltage at the cathodes of the EFP-60's other than capacitative feedthrough.

The circuits were tested with common input operation (the points labeled A connected together) which is the condition given in the the section on the complete flip-flop. However, the circuits can also be operated by applying trigger signals separately to the driving tubes. Circuit action was observed by using a Tektronix 517 Oscilloscope. It was necessary to observe the action of the fastest circuit by connecting it directly to the deflection plates of the cathode ray tube. The pulses were obtained from a Spencer-Kennedy 503 Pulse Generator. Double pulses, for the measuring of resolving times, were generated from single pulses by various transmis-

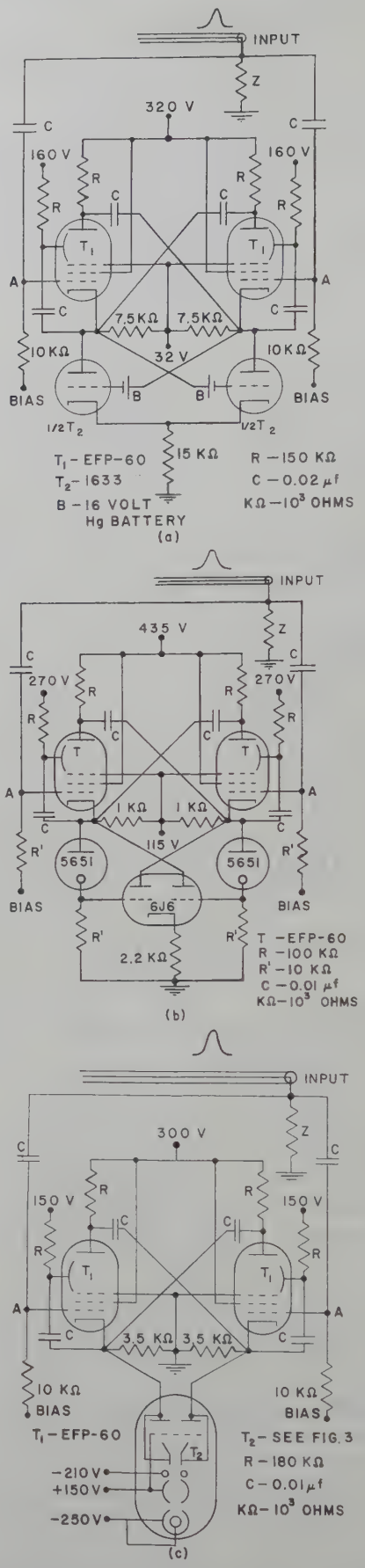

Fig. 5—Complete flip-flop circuits using (a) Battery flip-flop. (b) VR-tube flip-flop. (c) Bistable memory element as slave flip-flops.

sion line techniques. The duration of a pulse that will trigger the circuits and the resolving time for two such pulses is shown in Table I, below. The resolving time is the shortest time separation between the leading edges of two pulses such that the flip-flop changes its state for both pulses.

TABLE I

Circuit	Pulse Length	Resolving Time
5a	5 mμsec	10 mμsec
5b	2 mμsec	10 mμsec
5c	<1 mμsec	2 mμsec

The circuits, of course, are sensitive to supply and bias voltages because of the small voltage change between stable states and because of the dc coupling between driving tubes and the flip-flop tubes. The components of the circuits, including tubes, are not precision elements except for the plate resistors of the flip-flop tubes. The triggering pulses were approximately of the same amplitude as the V_f of the flip-flops. V_f could be varied between 6 and 10 volts by a suitable change in the plate-supply voltage and the plate resistors. Continuous operation could not be tested as there was no means of producing suitable triggering pulses at a high rate. There is, however, no reason to believe that the circuits will not operate at a frequency determined by the resolution time (consideration being taken of the allowable power dissipation of the EFP-60's) since there was no ringing at the plates of the flip-flop greater than 10 per cent of the voltage change.

Conclusion

An approach to the problem of designing high-frequency flip-flops has been shown in this paper and specific circuits have been developed to illustrate the method. It is not to be inferred that the circuits shown here could not be improved with respect to their high-frequency operation. It is quite probable that improvements could be made by designing tubes specifically for circuits operating on the principles shown in this paper. The beam deflection tube used as a slave flip-flop is a step in this direction.

No mention has been made of solid state electronic devices (crystal diodes and transistors). At present, they cannot compete with vacuum tubes in this application because the bandwidth of their characteristics is too narrow. That this situation may not exist for long, however, is indicated by recent advances in the development of these devices. A number of improvements could be made in the circuits shown in this paper if crystal diodes could be obtained with rectification efficiency close to 100 per cent at 100 mc.

Acknowledgment

We would like to acknowledge the assistance of Laszlo Monostori and Geoffrey Uyehara in the construction and testing of the experimental circuits shown in this paper and the help of Mrs. Susan Finnell Hart in the preparation of the manuscript.

A Topological Method for the Determination of the Minimal Forms of a Boolean Function*

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Summary—The topology of the n-dimensional cube is used to reduce the problem of determining the minimal forms of a Boolean function of n variables to that of finding the minimal coverings of the essential vertices of the basic cell system associated with the given function. The proof of this statement is contained in the central Theorem 4. A numerical easily programmed procedure is given with which it is possible to treat problems with a greater number of variables than has heretofore been practical. The procedure bypasses the determination of the basic cells (the prime implicants of W. V. Quine) and locates the essential vertices, from which in turn the irredundant and minimal forms are obtained.

Introduction

THE PROBLEM to be considered in this paper is the determination of the so-called minimal forms of the function $f(x_0, x_1, \cdots x_{n-1})$ of the two valued variables $x_0, x_1, \cdots x_{n-1}$. This problem has been treated with varying degrees of success by Shannon,[1] Aiken *et al.*,[2] Quine,[3] Lee,[4] Muller,[5] and others. The use of the n dimensional cube as a model is certainly not new. To the best of the author's knowledge, all attempts in this connection have been confined to very little else other than noting that a correspondence can be set up between the terms of the canonical form of f and the vertices of the n cube. The present exposition, based on the work of Quine[3] and Mueller,[6] makes effective use of this correspondence, and presents advances not considered by either of these writers. In order that this paper be as self-contained as possible, we shall redefine certain notions from elementary combinatorial topology and other fields.

If the function referred to above is expressed as a sum of products of n, or fewer variables, we shall call each such product a *term* of f. The operations *sum* and *product* are defined by the tables

+	0	1
0	0	1
1	1	1

·	0	1
0	0	0
1	0	1

In addition to these operations we shall make use of the operation prime (′) defined by

$$0' = 1$$
$$1' = 0.$$

It is well-known that every Boolean function $f(x_0, x_1, \cdots x_{n-1})$ can be expressed in terms of these operations in the canonical form

$$f(x_0, x_1, \cdots x_{n-1}) = \sum_{i=0}^{2^n-1} f_i x_0^{i_0} x_1^{i_1} \cdots x_{n-1}^{i_{n-1}}$$

where $i_0, i_1, \cdots, i_{n-1}$ are the binary digits of the number i and

$$x^0 = x', \qquad x^1 = x.$$

For the sake of definiteness we define a minimal form of f. It will be seen subsequently that the methods used for determining such forms do not preclude the making of other reasonable definitions.

A *minimal form* g of f is a sum of terms such that

1) $f = g$.
2) The combined sum of the number of + and · operations is a minimum.

The N-Dimensional Cube Model

In order to describe the procedure for determining the minimal forms of a given Boolean function f, we set up a one-to-one correspondence between the terms of the canonical form and the vertices of the unit n cube.

We regard the unit n cube as being made up of cells defined inductively as follows:

0-cell or *vertex*—a point,
1-cell—line segment without end points,
2-cell—quadrilateral without sides or vertices,
3-cell—hexahedron without vertices, edges, or faces.

The 3-cube, for example, can be considered as being made up of eight 0-cells, twelve 1-cells, six 2-cells, and one 3-cell.

The *k faces* of a cell are all of the k cells incident (immediately adjacent) with the cell. In Fig. 1 the 2-cell a is incident with the 1-cell c but is not incident with the 2-cell b.

By way of further example, a 2-cell has four 1-faces and four 0-faces. A 1-cell has two 0-faces.

A cell is said to *cover* a set of vertices if these vertices are 0-faces of the cell.

Making use of this terminology we now proceed to elaborate on the correspondence referred to in the first

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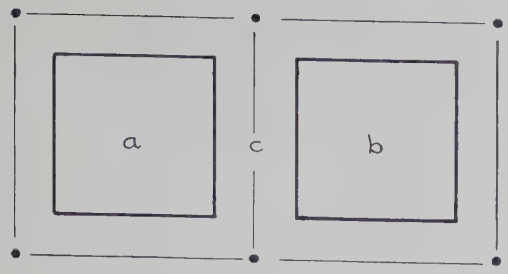


Fig. 1—Clarification of incidence.

paragraph of this section. We choose a coordinate system on the unit n cube with coordinates $(i_0, i_1, \cdots, i_{n-1})$ and to each vertex we make correspond the term $x_0^{i_0}x_1^{i_1}\cdots x_{n-1}^{i_{n-1}}$ of the canonical form of the given function. The decimal number $i_0+2i_1+2^2i_2+\cdots+2^{n-1}i_{n-1}$ will be called the vertex number of this vertex. We also set up the following correspondence between k cells and groups of terms of the canonical form:

k cell$\leftrightarrow$the sum of 2^k terms of the canonical form which correspond to all the vertices covered by the cell.

Of course, since the terms corresponding to the vertices covered by a k cell have $n-k$ variables in common, the above correspondence can be described as

$$k \text{ cell} \leftrightarrow \text{an } n-k \text{ variable term.}$$

We are now in a position to use interchangeably the algebraic and topological terminology.

The *cell-complex* of a given Boolean function is understood to be that subset of cells of the n cube whose members are defined as follows: a cell belongs to this subset if all of its 0-faces (a 0-face of a 0-cell is here taken to be the 0-cell itself) belong to the set of vertices of the function. For example, the cell-complex of the function

$$f(x_0, x_1, x_2) = x_0'x_1'x_2' + x_0x_1x_2 + x_0x_1x_2' + x_0x_1'x_2' + x_0x_1'x_2$$

consists of five 0-cells, five 1-cells and one 2-cell as indicated in Fig. 2.

The Basic Cell System

A *basic* cell of the cell-complex associated with a given Boolean function is one which is not a proper face of any other cell. (A *proper* face is any face but the cell itself.) In the example shown in Fig. 2 there are two basic cells, a 2-cell and a 1-cell.

The *basic cell system* of the cell-complex of a given Boolean function is that subset of basic cells of the given cell-complex.

It is the basic cells of the cell-complex which will be important in determining the minimal forms of the given function f. Corresponding to each minimal form g of f there always exists a set of cells covering the vertices of f which we shall refer to as a minimal covering. This covering is more precisely defined as follows:

A *minimal covering* of a subset of vertices S of an n-cube is that set of cells M such that

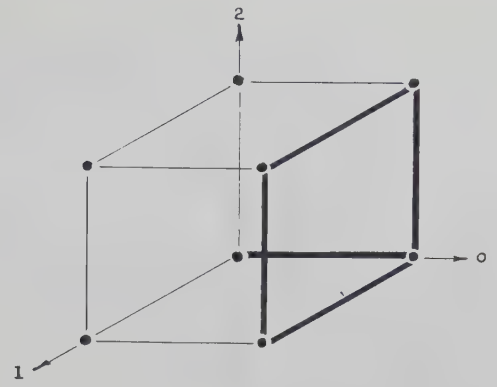


Fig. 2—A basic cell system.

1) M covers S.
2) The sum $\sigma = m+T-1$, where $T = \sum_{i=1}^{m} n-k_i$, is a minimum; m is the total number of cells of M, and k_i is the dimensionality of the ith cell.

The basic cells correspond exactly to what Quine calls "prime implicants" and the following is essentially Quine's Theorem 1.

Theorem 1

Every minimal covering consists of basic cells.

Proof: If there exists a minimal covering M containing a cell c which is not basic, then this cell is a proper face of some other cell c' of the cell-complex. Now consider the set of cells M' which are formed from M by deleting c and adding c', if it is not already in M. Since M' covers the same vertices as M, M' has the same or a smaller number of cells than M and $\sigma' < \sigma$; thus M cannot be a minimal covering. Hence M cannot contain a nonbasic cell and the theorem is proved.

This theorem enables us henceforth to confine our attention to the basic cell system. We proceed to define certain notions connected with this system before attempting to find minimal coverings.

The Irredundant Coverings

An *irredundant covering* I of the vertices of a given function is a set of basic cells of the basic cell system covering these vertices and having the property that if a basic cell of I were removed a vertex would be left uncovered by basic cells of I.

In the example of Fig. 2 the basic cell system is itself an irredundnat covering.

In Fig. 3 the coverings a, c, e; a, b, d, e; b, d, f; b, c, e, f; and a, f, c, d, are all irredundant.

Theorem 2

Every minimal covering is irredundant.

Proof: Assume that the covering M is minimal but not irredundant. It would then be possible to remove a basic cell c from M without uncovering any vertex. Now $\sigma = m+T-1$ is presumably a minimum. If a basic cell c of dimension S were removed from M then $m+T-1$ would become $m-1+T-1-(n-S) = m+T-1$

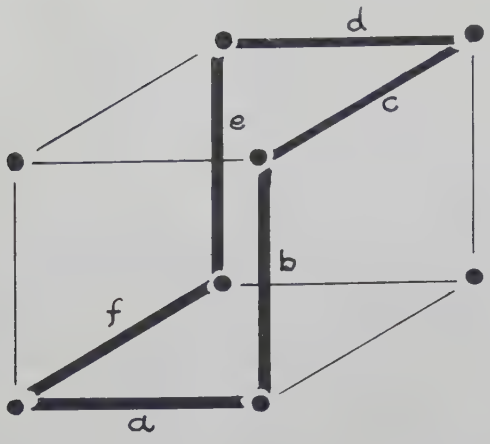


Fig. 3—Basic cell system with 5 irredundant coverings.

$-(n+1-S)<m+T-1$ thus producing a contradiction.

The above theorem enables us to get at minimal coverings by first finding all irredundant coverings. All minimal coverings can then be obtained by selection (in accordance with the definition on minimal coverings, or any other reasonable definition) from the set of irredundant coverings. With a view to obtaining all irredundant coverings, we make the following definitions.

The *basic star* of a vertex of the function f is the set of basic cells of the basic cell system which are incident with the given vertex.

A basic star is called *essential* if it contains no other basic star as a proper subset.

The vertex associated with an essential star will be called an *essential vertex.*

An *irredundant covering* of the set of *essential* vertices of a function is a covering of the essential vertices which has the property that if any basic cell were removed from this covering an essential vertex would be left uncovered. In connection with the stars just defined we have the following theorem.

Theorem 3

Every basic star contains an essential star.

Proof: If the basic star S is essential, the theorem is obvious. If S is nonessential, then S contains a basic star S_1. If S_1 is essential, the theorem is proved; if S_1 is not essential then it, in turn, contains a star S_2.

If we continue in this manner, we arrive at an essential star contained in S or we get a finite sequence of $k+1$ stars $S, S_1, S_2, \cdots, S_k$ each of which is properly contained in the preceding one. We must therefore conclude from the theorem on nested sets that the star S_k contains only one cell and is therefore essential.

The connection between the essential stars and the irredundant coverings of the basic cell system is contained in the theorem.

Theorem 4

Let I_e be the set of all irredundant coverings of the essential vertices of a given function and let I_f be the set of all irredundant coverings of the vertices of the given function f, then $I_e=I_f$.

Proof: Let i_e be any irredundant covering belonging to I_e. We wish to show that this covering is a member of I_f. We first show that i_e is a covering of the vertices of f. Suppose the contrary. Then some nonessential vertex P of the vertices of f must not be covered by i_e. The star at P contains an essential star emanating from some point P' and the cells of P' all cover P. Therefore P is covered by the cells of some essential star contrary to assumption. Thus, i_e is a covering of the vertices of f. Furthermore, if any cell of i_e were removed, a vertex would be uncovered. Therefore, i_e is an irredundant covering of the vertices of f and hence i_e belongs to I_f.

Now let i_f be any member of I_f. Our objective is to prove that i_f belongs to I_e. Certainly i_f is a covering of the essential vertices. We wish to show that it is an irredundant covering of these vertices. If i_f were not an irredundant covering of the essential vertices, then it would be possible to remove a basic cell from i_f without uncovering any essential vertex. The remaining basic cells still cover the essential vertices. If this covering is not an irredundant covering of the essential vertices, basic cells can be removed until it is. However, this last covering is an irredundant covering of all the vertices, (using the first part of this theorem, which we have proved). Thus we have removed basic cells from the irredundant covering of all the vertices i_f and we still have an irredundant covering left, which is impossible.

This theorem reduces the problem of determining the set of irredundant coverings of the vertices of f to that of determining the irredundant coverings of a smaller set of vertices, namely the essential vertices.

Numerical Procedure for the Determination of the Essential Stars

We consider in this section the construction of a numerical procedure for determining the essential stars of the basic cell system of a given function f. For this purpose we make use of the vertex numbers described in the second section. We take as point of departure the canonical form of the given function whose minimal forms are to be found and list the vertex numbers corresponding to each term of this function. We then choose any vertex of the function and find all basic cells emanating from this vertex. (The numerical procedure for accomplishing this will be described presently.) If there is only one such basic cell, then the star on this vertex is obviously essential. It is then unnecessary to consider any other vertex incident with this basic cell for it cannot produce another different essential star. We therefore delete from the set of vertex numbers of the given function all such vertex numbers and proceed to the next undeleted vertex number and determine the star on this vertex. When this process has been completed, any star which contains another is deleted and we finally arrive at the set of essential

stars. From this set of essential stars, we may select in accordance with some definition of minimality, the irredundant and the minimal coverings. The numerical procedure is based upon the theorems listed below.

Theorem 5

Let N be the vertex number of any given vertex of a unit n cube, then all of the opposite vertex numbers N_{qk},

$$q = 0, 1, \cdots \binom{n}{k} - 1$$

of all the k cells incident with N are given by

$$N_{qk} = N + \sum_{j=0}^{k-1} 2^{p_j}(-1)^{i_{p_j}}, \qquad q = 0, 1, \cdots \binom{n}{k} - 1$$

where $p_0, p_1, \cdots, p_{k-1}$ runs through all possible combinations (one combination corresponding to each value of q) of the numbers $0, 1, \cdots, n-1$; k at a time, and the i_{p_j} are the coordinates of N.

Proof: The vertex with vertex number N has the coordinates $(i_0, i_1, \cdots, i_{n-1})$. The coordinates of the opposite vertex of any k cell incident with this vertex can be obtained from this vertex by adding $(1 \oplus 1 = 0$ in this addition) k ones in all possible ways to this set of coordinates. Since the decimal form of N is given by $N = i_0 + 2i_1 + 2^2 i_2 + \cdots + 2^{n-1} i_{n-1}$ and since $i_p \oplus 1 = i_p + (-1)^{i_p}$ the stated result follows easily.

Theorem 6

If $N_{q,1}$; $q = 0, 1, \cdots, n-1$ are the opposite vertex numbers of all 1-cells incident with N, then the opposite vertex numbers of all $(k+1)$-cells incident with N are given by

$$N_{q,k+1} = N_{q_0,1} + N_{q_1,1} + \cdots + N_{q_k,1} - kN;$$
$$q = 0, 1, \cdots \binom{n}{k+1} - 1$$

where $q_0, q_1, \cdots, q_k$ are all combinations taken $k+1$ at a time from the numbers $0, 1, \cdots, n-1$.

Proof: The vertex number N together with the vertex numbers of the opposite vertices of all 1-cells incident with N are

$$N = i_0 + 2i_1 + 2^2 i_2 + \cdots + 2^{n-1} i_{n-1}$$
$$N_{01} = [i_0 + (-1)^{i_0}] + 2i_1 + 2^2 i_2 \cdots + 2^{n-1} i_{n-1}$$
$$N_{11} = i_0 + 2[i_1 + (-1)^{i_1}] + 2^2 i_2 \cdots + 2^{n-1} i_{n-1}$$
$$N_{21} = i_0 + 2i_1 + 2^2[i_2 + (-1)^{i_2}] + \cdots + 2^{n-1} i_{n-1}$$
$$\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots$$
$$\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots$$
$$N_{n-1,1} = i_0 + 2i_1 + 2^2 i_2 \cdots + 2^{n-1}[i_{n-1} + (-1)^{i_{n-1}}].$$

It is clear that if all possible sums $k+1$ at a time are formed from $N_{01}, N_{11}, \cdots, N_{n-1,1}$ and kN is subtracted from each sum that $N_{q,k+1}$,

$$q = 0, 1, \cdots \binom{n}{k+1} - 1$$

results.

Theorem 7

If c_1 and c_2 are two k cells of the unit n cube incident with the same vertex P and whose corresponding 1-faces extend in the same directions, then c_1 and c_2 are identical.

Proof: Assign directions $0, 1, \cdots, n-1$ to the 1-faces of the unit cube. There can be only one 1-face incident with P in direction 0. Hence, if c_1 and c_2 are not identical they must have this 1-face in common. Similarly, in direction 1 there can be only one 1-face incident with P; hence c_1 and c_2 have two 1-faces in common. Continuing this process leads to the conclusion that c_1 and c_2 have k 1-faces in common and are therefore identical.

With these theorems we now consider the problem of determining the irredundant and minimal forms of the function

$$f = x_0'x_1'x_2'x_3' + x_0x_1'x_2'x_3' + x_0x_1x_2'x_3' + x_0'x_1'x_2x_3'$$
$$+ x_0x_1'x_2x_3' \; x_0'x_1x_2x_3' + x_0x_1x_2'x_3 + x_0'x_1x_2x_3 + x_0x_1x_2x_3.$$

We write first the vertex number of the vertex corresponding to each term by simply reading the exponents of each term and converting to decimal, giving the set of vertex numbers 0, 1, 3, 4, 5, 6, 11, 14, 15.

To determine the basic cells emanating from any given vertex, we choose any one of the given vertices, say 5, and find the opposite vertex numbers of all 1-cell incident with 5. If these numbers are present in the above set, then 1-cells connecting 5 and these numbers are part of the cell-complex for this function. We next examine these 1-cells in pairs to decide on whether or not they are faces of 2-cells and then examine all 2-cells in triplets, etc.

A systematic method for accomplishing this is indicated in the following.

List the vertex number in question in decimal and in binary together with the remaining vertices as indicated below and assign numbers 0, 1, 2, and 3 to the four directions in which the 1-cells can emanate.

0	1	2	3		5
1	2	4	8		
				0	(02)
				1	✗
				3	
				4	∅
1	0	1	0	5	
				6	
				11	
				14	
				15	

Using Theorem 5 enter the direction number in the proper row under vertex 5 if there exists a 1-cell in this direction whose opposite vertex is one of the vertices of the given set. The use of Theorem 5 is facilitated if the numbers 2^0, 2^1, 2^2, 2^3 are listed above the binary equivalent of the vertex 5. Then to get all possible opposite vertices of 1-cells emanating from 5, read the binary equivalent from left to right and subtract from 5 the number above if this binary number is 1 and add if 0. Thus it is seen that there exist two 1-cells emanating from 5 in directions 0 and 2 and with opposite vertices at 4 and 1 respectively.

Next we must decide whether or not members of this pair of 1-cells are faces of a 2-cell; for this we use Theorem 6. The opposite vertex number is $4+1-5=0$ which is present in the given set, therefore, there is a 2-cell emanating from 5 with opposite vertex at 0 and having directions 0 and 2. Since the 1-cells in directions 0 and 2 are faces, we cross these out and enter 02 in row 0 and circle it, indicating that this is a *basic* cell. If there is only one basic cell emanating from 5, as this particular example shows, then we need not carry out this process for the remaining vertices 0, 1, 4 of this basic cell since these vertices cannot carry any other essential stars. We then eliminate these vertices from the given set and repeat the process for the remaining vertices. This gives the table below. The circled numbers under each vertex number represent all the basic cells emanating from that vertex, that is, the basic star associated with the vertex. This table then represents a set of stars from which the essential stars are obtained. Any star which contains another is eliminated and the remainder is the set of essential stars.

0 1 2 3										
1 2 4 8		ø	✗	3	✗	5	6	11	14	15
0 0 0 0	0					⓪②				
1 0 0 0	1			①		✗				
1 1 0 0	3							③		
0 0 1 0	4					ø	①			
1 0 1 0	5									
0 1 1 0	6								③	
1 1 0 1	11			ø						②
0 1 1 1	14						ø			⓪
1 1 1 1	15							②	ø	

It is to be noted that certain basic cells appear more than once in the above array of circled numbers. For example, the basic 1-cell emanating in direction 3 from 6 with opposite vertex at 14 is clearly the same as that emanating in direction 3 from 14 and with opposite vertex at 6. (Also follows from Theorem 7.) If Theorem 7 is used to detect all such repetitions, we have the above array, where the undeleted circled numbers represent basic cells no two of which are identical. If these cells are renumbered 1 through 7, by numbering the cells in each column and proceeding columnwise from left to right, we have the following array for the stars on each vertex.

3	5	6	11	14	15
1					
	2				
		3			
4			4		
		5		5	
			6		6
				7	7

It is now easily seen that all of these stars are essential. Therefore, according to Theorem 4, any selection of rows having the property that all columns are represented and also having the property that if any row of the selection is omitted a column will not be represented—is an irredundant covering. The 2nd, 4th, 5th, and 6th rows make up such a selection. The basic cells in this irredundant covering are thus 2, 4, 5, 6. Other irredundant coverings in this problem are 1, 2, 3, 6, 7; 1, 2, 5, 6; 2, 3, 4, 7; 2, 4, 5, 7. All these coverings except 1, 2, 3, 6, 7 according to our definition are also minimal. The basic cell 2, according to the 1st array, covers the vertices with coordinates (0, 0, 0, 0), (1, 0, 0, 0,), (0, 0, 1, 0), (1, 0, 1, 0). Its algebraic term representation is thus $x_1'x_3'$.

Continuing in like manner with the remaining basic cells of the above coverings, we have the two minimal forms:

$$f = x_1'x_3' + x_0x_1x_2' + x_0'x_1x_2 + x_0x_1x_3$$

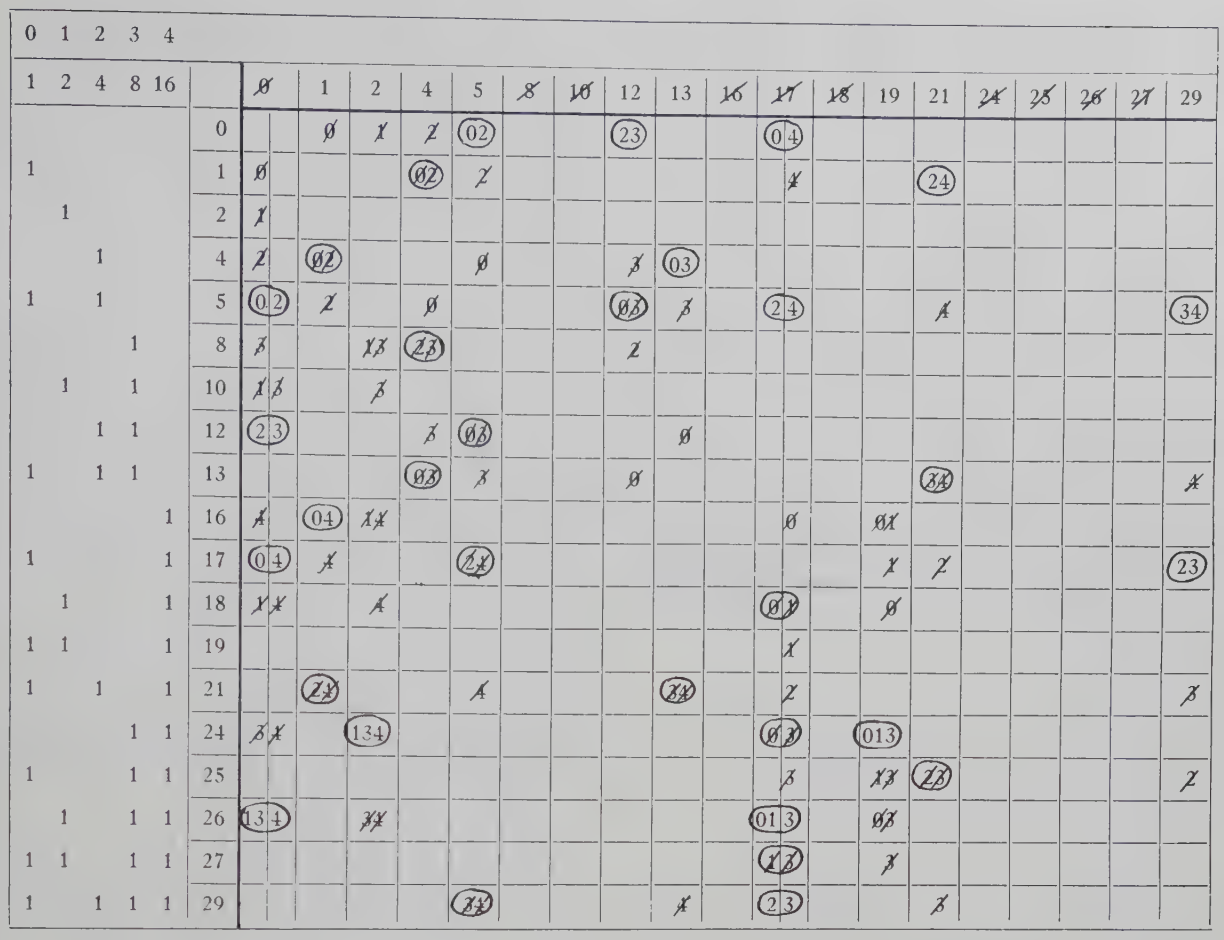
and

$$f = x_1'x_3' + x_0x_1x_2' + x_0'x_1x_2 + x_1x_2x_3.$$

As a second example, consider the problem of determining the irredundant and minimal forms for the function whose vertex numbers on the 5-cube are:

0, 1, 2, 4, 5, 8, 10, 12, 13, 16, 17, 18, 19, 21, 24, 25, 26, 27, 29.

This function produces the following array. We have made use of Theorem 7 in cancelling such duplications as 23, 03, 34 etc. The 2-cells with opposite vertices 29, 5, and 21, 13 are seen to be identical since they have the same direction 34 and are both incident with vertex 5.



The computation was carried out beginning with vertex 0 and proceeding in the direction of increasing vertex number. If columns headed 2 and 19 had been computed first, some labor would have been avoided, for the 3-cells incident with these vertices are incident with vertices 0 and 17.

There are a total of 9 different basic cells represented, which we proceed to number 1, 2, · · · , 9, giving the following listing of stars.

1	2	4	5	12	13	19	21	29
1								
	2							
3		3	3					
		4		4				
		5	5	5	5			
						6		
7			7				7	
			8		8		8	8
							9	9

The star on vertex 4 is seen to be nonessential since it contains the star on vertex 12. Similarly, the star on vertex 5 is nonessential since it contains the star on 13. Also the star on 21 contains that on 29. Deleting all nonesssential stars gives the following listing:

1	2	12	13	19	29
1					
	2				
3					
		4			
		5	5		
				6	
7					
			8		8
					9

Since 2 and 6 must be chosen in any irredundant covering, this reduces to:

1	12	13	29
1			
3			
	4		
	5	5	
7			
		8	8
			9

from which we choose irredundant coverings. Each such covering taken with basic cells 2 and 6 is an irredundant covering of the essential vertices and therefore of the original set of vertices of the given function. These coverings are

2, 6, 1, 4, 8
2, 6, 3, 5, 9
2, 6, 1, 5, 8
2, 6, 7, 4, 8
2, 6, 1, 5, 9
2, 6, 7, 5, 8
2, 6, 3, 4, 8
2, 6, 7, 5, 9
2, 6, 3, 5, 8

Each covering in the above list is also minimal.

Conclusion

The significant features of the above exposition are as follows:

1) The determination of the irredundant and minimal forms does not depend on listing all the basic cells of the basic cell system, although the above procedure will give this system if desired (that is, the set of prime implicants in W. V. Quine's paper).[3]

2) The determination of irredundant and minimal forms of a given function is made to depend upon the determination of irredundant and minimal forms of a function with a smaller number of terms (namely the function corresponding to the set of essential points).

3) The above offers an easily programmed numerical procedure for obtaining these forms as well as an easily visualized model for further study.

4) Problems involving more variables than have previously been possible present no difficulties with this method.

Further work is being done on the problem of devising shorter methods of selecting the irredundant and minimal coverings from the set of essential stars. This work, together with programming procedures for a digital computer will be presented in a later report.

Acknowledgment

The authors wish to acknowledge the considerable assistance of Lts. S. Petrick and F. E. Starr, both of the Applied Mathematics Section of the Computer Laboratory, Air Force Cambridge Research Center. The proofs of most of the theorems presented here were formulated during many productive discussions with these men.

Logic Circuits for a Transistor Digital Computer*

G. W. BOOTH† and T. P. BOTHWELL†

Summary—**The reliability and performance which can be achieved in high-speed switching circuits using presently available high-frequency junction transistors suggests the use of transistor circuits in preference to more conventional circuits for many applications. The area of airborne digital computers is one in which the physical characteristics of the transistor as well as of associated low dissipation components can be most favorably exploited. We have presented here a group of circuits which fulfill the requirements of speed, low dissipation, size, and weight for most such applications. The circuits shown will operate over the range −30°C to +60°C, and actually have been operated over the range −50°C to +90°C. Low dissipation of the circuits places minimum requirements on power supplies, and temperature control may be achieved with only a small amount of cooling. An estimate can be obtained from an example. For a large-scale computer, say 2000 transistors, 800 of which are in bistable circuits, total dissipation will be less than 140 watts.**

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Introduction

ONE of the important properties of a digital computer is that it may be assembled simply and easily from a few well-chosen functional circuits. Each of these circuits represents a logical element that is useful to the system or logic designer in planning a computer. The evolution of a set of standard logical circuit blocks allows this design without direct reference to the circuits, thus reducing logic design to the application of a set of rules expressing the input and

output capabilities of each of the logical circuit blocks. The responsibility falls upon the circuit designer to provide blocks that will result in an efficient logic design and a reliable equipment. In fact, the efficiency with which a computer may be designed and its reliability of operation are the principal criteria for determining success or failure of a group of circuits.

From the view of manufacturing economy and maintainability, it is obviously desirable to minimize the number of different types of blocks. In a large scale machine, where these circuits are used many times, the individual circuits must exhibit extremely high orders of reliability. Moreover, this reliability must be achieved almost invariably under difficult environmental conditions—variations in temperature, vibration, noise pickup, etc. While all this leads to an extremely conservative approach to circuit design it is nevertheless important to realize that the use of too many components in an effort toward conservatism may defeat itself because of the increased catastrophic failure probability. The circuit designer must choose the appropriate middle ground.

This paper presents a group of transistor circuits for a general computer application designed with the above considerations in view.[1] The circuits described are the result of a conservative design approach which takes advantage of the high switching efficiencies obtainable with the alloy junction transistor. Precision resistors (1 per cent) are used throughout, yet are treated as 5 per cent resistors in the design. Power dissipation, current, and voltage levels are kept low in diodes and transistors, yet are large enough to avoid serious problems due to noise pickup. Circuit dependence on individual parameters of the transistors is minimized. Commercially available high-frequency alloy junction transistors are used and a considerable "slump" of transistor gain from specified values can be tolerated without sacrificing performance. The circuitry under discussion is capable of serial operation at 250 kc, and, with redesign, can be increased to 500 kc. Temperature stability is sufficient to assure circuit operation between $-30°C$ and $+60°C$; actually the circuits have been operated successfully between $-50°C$ and $+90°C$. In fact, in 60 hours of operation of a counter at $+80°C$, no deterioration in circuit performance or transistor characteristics was detected.

The two basic circuits are a bistable multivibrator, or flip-flop, and a gated pulse amplifier. All information flows in the form of 0.5 microsecond pulses through chains of one or more gated pulse amplifiers and is ultimately stored in a flip-flop. Gate control information is in the form of dc levels from flip-flops, in most cases without intermediate amplification. The symmetry of the flip-flop output, plus the fact that information is never generated in the form of dc levels, eliminates the requirement for an inverter in the system. For the few cases where a flip-flop is required to control a large number of gates, a dc amplifier is provided. Similarly, for the case where an information pulse or time pulse must be distributed to a large number of gates, a pulse power amplifier is used.

Description of Circuits

Flip-Flop

Considerable effort was devoted to the selection and design of the flip-flop. The Eccles-Jordan circuit type, shown in Fig. 1, was chosen because of its complementary outputs, its designability, and because of the efficient operation afforded by "saturation" operation of the transistors. The limited frequency response available in alloy junction transistors requires clamping of the turn-off transient for fast "rise" times under load. Collector current in the flip-flop transistors is limited to 10 ma in order to allow conservative use of the transistors. A collector output swing of 6 volts was chosen as large compared to diode forward voltage drops, yet small compared to breakdown voltages of diodes and transistors.

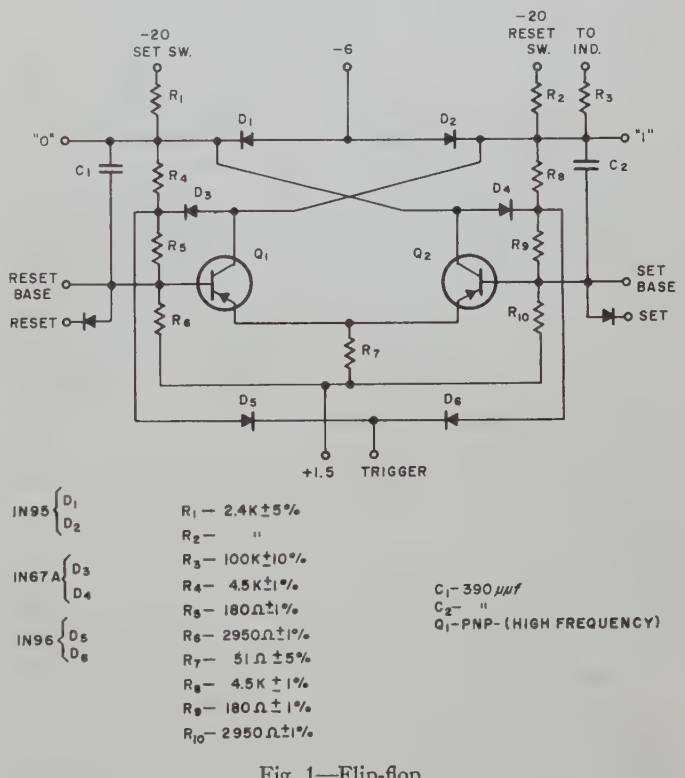


Fig. 1—Flip-flop.

The flip-flop was designed with the following primary considerations in view; dc stability, switching speed,

[1] Circuits for similar applications have been described by the authors and others, T. P. Bothwell, G. W. Booth, and E. P. English, "A Junction Transistor Counter with High Speed Carry," "Transistors I," RCA Labs., Princeton, N. J., pp. 646–660; March, 1956.
D. E. Deuitch, "A Novel Ring Counter Using Junction Transistors," "Transistors I," RCA Labs., Princeton, N. J., p. 640; March, 1946.
E. W. Sard, "Junction transistor multivibrators and flip-flops," 1954 IRE Conv. Rec., part II, pp. 119–124.
C. L. Wanlass, "Transistor circuitry for digital computers," IRE Trans., vol. EC-4, pp. 11–16; March, 1955.

load requirements, stability margins, small trigger power, and fast circuit recovery after trigger. The design of the dc circuit parameters was carried out to assure that a 2 ma load specification was met, as well as to assure stability under conditions of large I_{co} and against triggering by small noise pulses.[2] Reverse bias on the base emitter diode of the nonconducting transistor is guaranteed with allowances for I_{co} and leakage in diodes of at least 120 microamps, which corresponds to the I_{co} which might be encountered at +60°C. Actually, for most cases, much greater I_{co} than this will still result in cutoff bias, since this figure is based on tolerance extremes of all components.

The design assures saturation in the "on" transistor for worst cases of all resistor and supply voltage tolerances for transistors with large-signal current gains greater than 15. No maximum gain need be specified.

A few of the other important factors in the design might also be discussed at this time. The relation between loading and switching speed as a result of the use of the clamp can readily be determined. When the conducting transistor turns off, its collector rides toward some potential which is less than the supply voltage. In a flip-flop of this type the "aiming" potential must be greater than the clamp voltage in order to maintain dc stability under load conditions. The aiming potential is defined as the resultant potential at the cutoff collector due to the divider action of the collector resistor, the feedback resistor, and the load resistor when the clamp diode is disconnected. However, to assure that worthwhile advantage in speed is obtained, the aiming potential to clamp voltage ratio must be somewhat greater than unity. For the circuit of Fig. 1, with a 2 ma load current, this ratio is 1.5.

The feedback capacitor C_f (C_1 or C_2 in Fig. 1) was chosen empirically to perform speedup and memory functions for a typical pair of transistors. Too large a C_f resulted in slow switching at the cutoff collector. Too small a capacity resulted in tight frequency response requirements on the transistors for a satisfactory range of trigger pulse voltage and width. A compromise in the vicinity of 400 $\mu\mu$f gave a feedback coupling which was relatively independent of transistor characteristics.

To achieve a high repetition rate for the flip-flop, the discharge time constant (τ) of the feedback capacitor should be as small as possible. This time constant is given by

$$\tau = C_f\left(\frac{R_b\ R_f}{R_b + R_f}\right)$$

where, referring to Fig. 1:

C_f is either C_1 or C_2,

R_b is either R_6 or R_{10},

and

R_f is either $(R_4 + R_5)$ or $(R_8 + R_9)$.

To maintain high frequency loop gain C_f must be increased if R_f is reduced. R_f is largely determined by current levels in the circuit and hence is not readily varied. Thus for a minimum resolution time we see that it is desirable to have R_b as small as practicable.

A common emitter resistor, R_e, (R_7 in Fig. 1) is included to obviate the need for a small bias supply voltage. With R_b small, the bias potential to which R_b is returned must be small to maintain adequate "on" current into the base of the conducting transistor. Such small bias voltages are both difficult and inconvenient to generate and regulate. For this reason a bias is generated by the saturation current of the "on" transistor through R_e. In the particular circuit used here, the emitter return was chosen as +1.5v in order that the collector of the conducting transistor be assured to be positive with respect to ground, thus assuring a reverse bias on ground returned gates, etc.

A pulse steering arrangement was incorporated into the circuit to reduce saturation effects of the "turn-on" trigger pulse at large trigger amplitudes. A feedback diode from each collector to a tap on the feedback resistor, as shown in Fig. 1, serves to provide a shunt path from this base tap to the collector of the conducting transistor.[3] Hence a large amplitude trigger does not cause a high degree of saturation in the conducting transistor. On the cutoff transistor, the feedback diode is reverse biased by 6v, hence has no effect on circuit operation. It should be noted that this feedback diode, as used in this circuit, does not provide an antisaturation clamp, since some fixed current will flow through the resistor between feedback diode and base for the essentially constant forward bias drop of the diode. For a high gain transistor, this fixed current may represent saturation; for a low gain transistor it may not. However, if the gain of the conducting transistor is sufficiently low as to cause it to be out of saturation by more than a few tenths of a volt, the feedback diode cuts off, providing maximum base current in the conducting transistor. Thus dc stability is not sacrificed by the use of the feedback diodes; in fact, the limiting dc stability conditions are unaffected by this circuit modification.

For the specific circuit shown in Fig. 1, a range of trigger amplitude of from 2.1 to 4.5v was obtained for a resolution time of 1.2 μsec. Operation with a trigger pulse width from 0.4 to 0.9 μsec at the 2.6v nominal pulse amplitude was achieved, under maximum symmetrical load, *i.e.*, 3000 ohms and 220 $\mu\mu$f in parallel on both sides. These results hold for all transistors which meet the specifications outlined at the end of this sec-

[2] This design was carried out in a manner similar to that described by T. P. Bothwell, "Design of Non-Saturating Junction Transistor Flip-Flop," presented at the AIEE Winter General Meeting; January, 1955.

[3] A diode "feedback" configuration similar to that employed here, but used specifically to prevent saturation in the steady state, was described by J. Warnock, in a talk entitled "Junction Transistor Switching Circuits," presented at the AIEE-IRE Joint Transistor Conference, Philadelphia, Pa.; February 19, 1954.

tion. Considerably wider limits were obtained for a typical pair of transistors.

Gated Pulse Amplifier

The second basic logic circuit is the gated pulse amplifier shown in Fig. 2. The gating function of the circuit is controlled by the "or-and" diode gate in the base lead of the transistor. Each "or" input of this gate is derived from a flip-flop whose output is 0 or −6v. A 2.6v positive pulse, biased at −6v is applied at the emitter. A pulse output will appear only if the base potential is more negative than −3.4v since, unless this condition is met, the base emitter diode will never be forward biased. This condition can exist when all "and" inputs have at least one "or" input at −6v. If one "and" input is at ground, the voltage division between its associated resistor (R_1, R_2, R_3) and R_5 will raise the base to −3v. More than one "and" input at ground will make the base more positive.

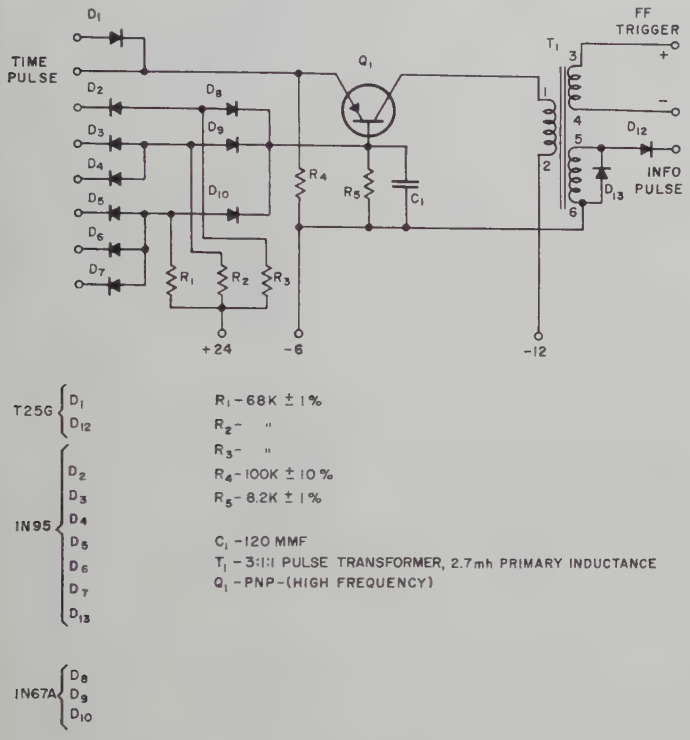


Fig. 2—Gated pulse amplifier.

When the gated pulse amplifier is primed we may neglect the diode gate and consider only the pulse amplifying qualities of the amplifier. The transistor is driven from zero bias to saturation by a 0.5 μsec pulse applied at the emitter. The capacitor C_1, Fig. 2, offers an increase in effective frequency response by allowing the circuit to operate as grounded base during the 0.1 μsec turn-on and turn-off period of the transistor. During the rise of the pulse, the transient current in the base lead is determined by the size of C_1 and the low pulse source impedance in series with the transistor base and emitter resistance. During the fall, the capacitor provides a low impedance in the base lead to diminish the effects of storage. Each of these transient effects are settled in approximately 0.1 μsec and therefore have little effect on the circuit during the flat-top portion of the pulse.

During the flat portion of the pulse the transistor is operating in saturation where the voltage drop from emitter to collector is negligible and $\beta I_B > I_c$. In this condition, a constant voltage appears across the load and the magnetizing current in the output transformer increases linearly. The pulse output will collapse if βI_B becomes less than I_c or if the pulse falls at the input. Either case will cause a high collector impedance to be presented to the load. The primary inductance of T_1 (Fig. 2) is chosen such that the output pulse width is a function only of the input pulse width. The diode (D13, Fig. 2) provides a low resistance path to damp the overshoot of the transformer at the end of the pulse. The design of the circuit shown in Fig. 1 allows for a 250 kc pulse repetition rate. A more thorough investigation of the effects of magnetizing current in iterative circuit operation has been carried out but is beyond the scope of this paper.

The gated pulse amplifier may be considered the amplifying element between output and trigger input of the flip-flop. From such a viewpoint, it can be seen that some minimum power gain (dc to pulse) is required in order to be able to pyramid gates and flip-flops in logical sequences. The greater the power gain, the broader the logical structure which is available to the logic designer, *i.e.*, the greater the number of gates which may be controlled by a flip-flop, or conversely the greater number of flip-flops which may be triggered by a single gate. Since the ratio of collector current to base current in the pulse amplifier may not be greater than the current gain β, the output current of the diode gate sets a maximum value of the gate collector current. Hence, the current output of the gate-amplifier is limited by the maximum load current which may be drawn from the flip-flop inputs to the diode gate, since the current drawn at each input is roughly equal to the diode gate output current. A less clearly defined relationship exists between the trigger pulse power required for the flip-flop and the load current available from it, but in general an increase in load current requires an increased trigger power, other circuit considerations (rise time, output voltage, etc.) being equal.

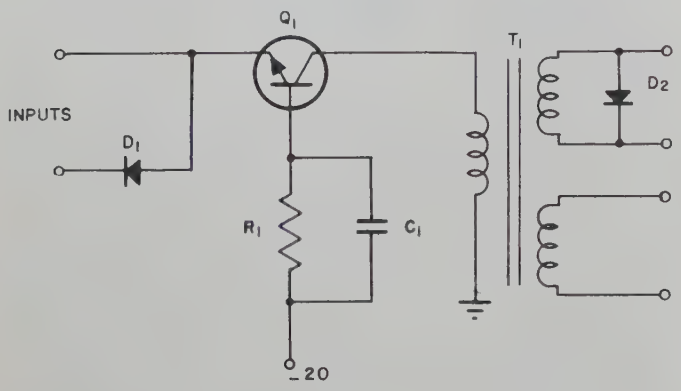
Considering the back current of the "and" diodes and the charge time constant of the capacitor in the base, the diode gate current was selected as 0.5 ma per input. Then, on the basis of breakdown voltages of available transistors (>20v), a minimum transistor current gain of 20, and assurance that the transistor operates in the saturation region, a power output of 30 mw could be obtained from a pulse amplifier. This was sufficient to trigger at least two flip-flops. Since each flip-flop is capable of delivering 2 ma to a load from each collector, four gate inputs may be loaded on each output. (A summary of the load capabilities and input require-

ments of each circuit is given below in the section on Application Rules.)

Amplifiers and Indicator

Two amplifiers complete the system, one a power pulse amplifier, the other a dc amplifier.

The power pulse amplifier is basically similar to the gated pulse amplifier, with the exception that no gating bias was provided and an *n-p-n* transistor was used in order to obtain a high power output. For a given emitter current, power output is proportional to collector voltage, and maximum collector voltage on the available *n-p-n* was considerably higher than on the available *p-n-p*. The circuit for this amplifier is shown in Fig. 3. A group of "or" diodes are provided in one output secondary for isolating a number of common loads. This amplifier is capable of providing a 180 mw pulse output for a 30 mw pulse input.

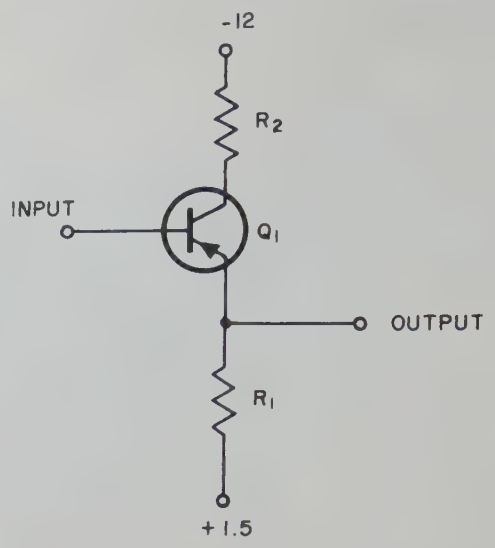


D_1 – T 25 G
D_2 – IN 96
R_1 – 6·8K ± 10%
C_1 – 560 $\mu\mu f$
T_1 – 9:1:1 PULSE TRANSFORMER
Q_1 – NPN-(HIGH FREQUENCY)

Fig. 3—Power pulse amplifier.

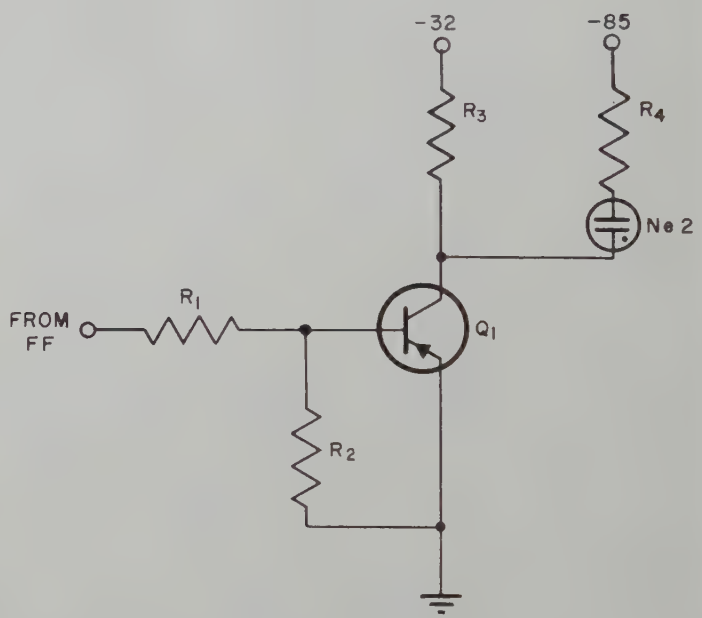
The dc amplifier (Fig. 4) is of the emitter-follower type, providing current gain with unity voltage gain. To prevent excessive dissipation and to avoid saturation in the transistor, a collector load resistor was introduced. Maximum transistor dissipation was calculated to be 40 mw and maximum load current was 18 ma. A voltage loss of <0.5v was experienced in this amplifier.

Although not necessary to the logic, an indicator is desirable for any test of the system and for trouble shooting. The indicator shown in Fig. 5 employs a biased neon tube which is switched off and on by an audio frequency transistor. Transistor requirements are that collector breakdown be greater than 35v, and current gain greater than 10. Dissipation in the transistors is negligible since only the "on" current of the neon lamp need be supplied. Neon tube requirements are more strict; extinguishing potential must be greater than 55v and firing potential must be less than 85v.



R_1 – 3.3 K ± 10%
R_2 – 330 Ω ± 10%
Q_1 – PNP (HIGH FREQUENCY)

Fig. 4—Emitter follower (dc amplifier).



R_1 = 100 Ω
R_2 = 10 K
R_3 = 47 K
R_4 = 100 K
Q_1 = PNP-(AUDIO)

Fig. 5—Indicator circuit.

Transistor Requirements

Transistor requirements for these circuits are modest enough that 85 per cent of the high frequency *p-n-p* transistors purchased from one manufacturer were

acceptable in all respects. The 15 per cent rejects were primarily due to high leakage at 20v. Although such transistors were operable in the circuits, the low output impedance was taken as an indication of a poor junction, with adverse implications on long-term transistor life. Complete specifications have been formulated along with the test circuits to determine the specifications, but are too lengthy to cover here. The basic requirements are listed below:

1) Frequency response (grounded base) >4 mc.
2) Large signal current gain (β) >15 at $I_c=10$ ma for FF; >30 at $I_c=10$ ma for GPA.
3) Collector leakage (I_{co}) <3 μa at 6v (25°C.); <6 μa at -20v (25°C.); $I_e=0$.

Application Rules

Table 1 summarizes the minimum output specifications for the circuits described in this report. It should be noted that the gated pulse amplifier (GPA) has two types of input; *i.e.*, one requiring a 2.6v, 3 ma, 0.5 μsec pulse, the other requiring a 6v, 0.5 ma level. Hence the outputs of the gated pulse amplifier (GPA) and power pulse amplifier (PPA) can drive only the pulse inputs of a GPA. On the other hand, the outputs of the flip-flop and emitter follower (FF and EF) can drive only the level (diode gate) inputs of the GPA. The emitter follower was designed to drive a maximum of 36 GPA inputs, but this restriction was a matter of design convenience and not fundamental to the circuit. Maximum pulse repetition frequency for the GPA is 250 kc. The flip-flop may be set and reset at a 500 kc rate; maximum triggering rate is 400 kc.

TABLE I

OUTPUT SPECIFICATIONS

Circuit Type	Output	
	Form	Maximum Load
GPA	2.6v Pulse 1/2 μsec (10 ma)	2—FF or 3—GPA or 1—PPA
PPA	2.6v Pulse 1/2 μsec (55 ma)	11 FF or 17 GPA or 7 PPA
FF	6v Level (2 ma)	4 GPA or 2 EF } +1 Ind.
EF	6v Level (18 ma)	36 GPA

LOGIC TECHNIQUES

The preceding sections have described the circuits with which the logic designer may work. The binary counter shown in Fig. 6 will serve to illustrate the type of logical structure to which the circuitry lends itself.

When a "count" is added to a binary counter, each bit is complemented according to the following two rules. Complement if:

1) The next least significant bit is "1" before addition of the count.

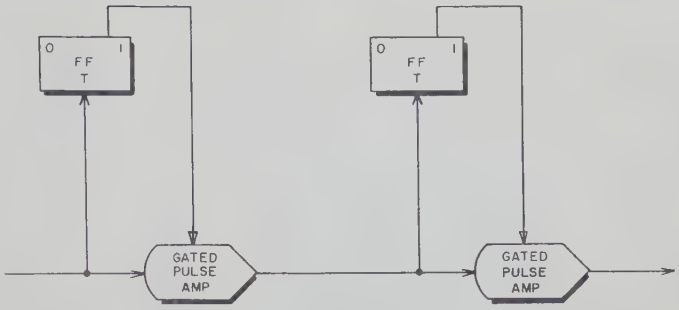


Fig. 6—Two stages of binary counter with high speed carry.

2) All less significant bits are complemented under rule 1. (The least significant bit is always complemented.)

Hence, all bits of a counter are complemented starting from the least significant bit and continuing through the first bit in which a zero is found to be stored. This function is performed by the chain of gated pulse amplifiers (Fig. 6). The trigger pulse will pass from the first to the second stage and complement the second flip-flop only if the first flip-flop was in the "1" state before the trigger occurred. It is important to note that although the state of the flip-flop may change as a consequence of the pulse the gated pulse amplifier acts on its initial state. This is due to the relatively slow rise of the flip-flop to the -3v level required to affect the output of the diode gate.

Since the carry propagation of the counter is independent of the switching time of the flip-flop, very fast carry "ripple" can be achieved. The circuit described here results in a 30 millimicrosecond carry ripple time per stage. Hence in a 12-bit counter, the longest carry time will be 0.36 μsec. Time required for the result to be available is longer than this by the settling time of the last flip-flop.

With very little additional equipment, the counter of Fig. 6 becomes a reversible counter. Fig. 7 shows the logic for a simple version. Here the "chain-gate" logic performs both complementation and binary count. When subtraction from the original count is desired, the counter is complemented as in Fig. 7 by the complement pulse and flip-flop, triggered with the count pulse, and recomplemented to be read. Three characteristics of the counters shown might be highlighted for general logic applications:

1) The pulse delay encountered through the gated pulse amplifier is small enough to allow a rather lengthy chain of amplifiers to be used with a minimum delay in passage through them.
2) The gated pulse amplifier allows a wide variety of logic due to the "or-and" cascade and the ability to use these circuits in an iterative connection.
3) The relationship of the flip-flop resolution time and pulse width allows the flip-flop to be read and changed in state with the same pulse.

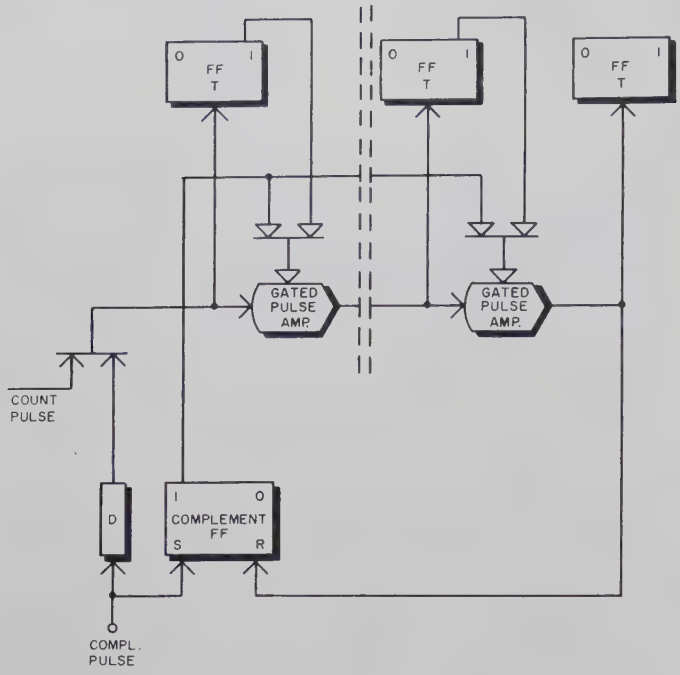


Fig. 7—Modification of binary counter to allow complementation and reversible counting.

Operating Experience

The proper test of circuits for digital computer use is their actual operation in a computer. To answer this need, RCA has a general purpose computer, specifically designed as a test facility. It has a high-speed random access magnetic core memory with a capacity of 1024 seven-bit characters and uses a Flexowriter for input-output. The installation is shown in Fig. 8.

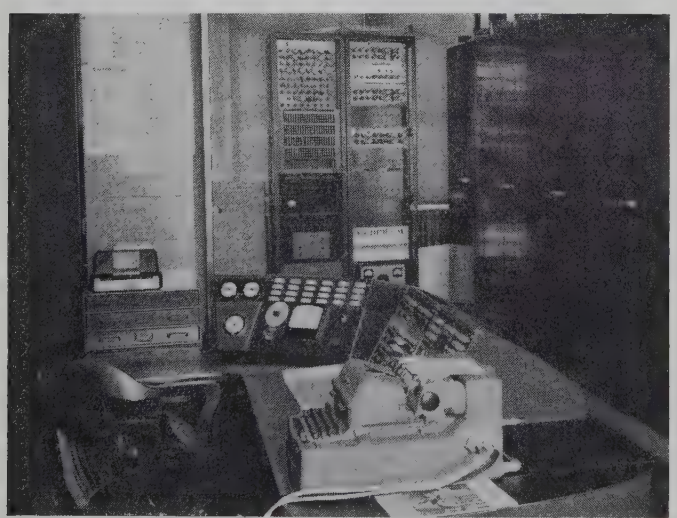


Fig. 8—Test computer showing transistor adder and multiplier counter installations in background.

Using these transistor circuits two components have been constructed for test in this machine. The first of these was a reversible counter and associated logic for keeping track of iterations during the multiply instruction and was built with a simple breadboard construction. Twenty-three transistors and 81 diodes are used. Marriage between machine and transistor circuits was performed by a group of vacuum tube amplifiers, pulse shorteners, etc. The unit has operated without error for over 450 hours of computer operation. Routine testing of transistors during shutdown did indicate progressive deterioration of a group of transistors, all of one manufacturer. Since these have been replaced with another type no further deterioration has been encountered.

An "adder, excess-three-converter" unit for the test computer was constructed as the second test component. Fig. 9 is a block diagram of the adder converter. This

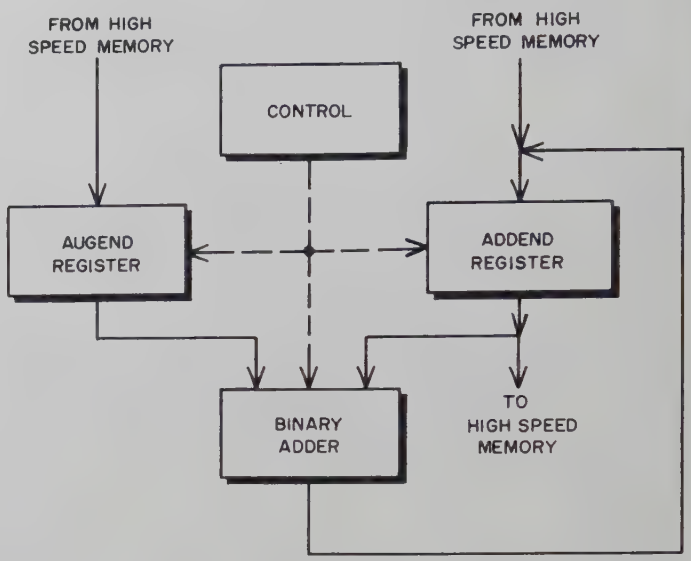


Fig. 9—Block diagram of "adder-excess three converter" test unit.

equipment was paralleled with the existing vacuum tube arithmetic unit. The results computed by the transistor equipment are substituted for those computed by the vacuum tube adder, and a parity check is made between the two results. The adder operates on the 20 μsec memory cycle of the test computer, and performs all functions of the "add" cycle in one-half of this period. The excess-three conversion is performed during the second half-period. Actual "add" time is 6 μsec, during which time two operands can be read into the operand registers, addition of these two performed, and the sum transferred back to one operand register in preparation for the excess-three correction.

The basic circuits for this equipment were laid out on 5 types of individual plug-in units. A total of 81 such plug-ins are used, containing 110 logical and 20 indicator transistors and 450 diodes. To date 670 hours of operation have been logged on this unit since debugging, with no diode failures, and a single transistor failure due to excessive leakage. It may also be noted that for higher temperature operation, these circuits may be adapted in alloy junction transistors when and if they become available.

Acknowledgment

The authors wish to acknowledge the contributions of their co-workers, W. A. Helbig and L. Kolodin, in the design of the circuits described.

Correspondence

Unit-Distance Binary-Decimal Codes for Two-Track Commutation*

In a recent letter to the editor[1] Bernard Lippel describes a decimal code for analog-to-digital conversion which has the property that only two commutator tracks (zones) are required for each decimal-digit decade being converted from shaft position into digital form. For brevity, we shall designate codes having this property "Lippel codes."

Three bits of the Lippel code representation of each decimal digit are obtained from a single track (zone), which has its brushes displaced angularly so that they contact the same track at different points. A fourth brush is used on a separate track to read the fourth bit of the coded representation.

The specific code that Lippel describes is not of unit distance.[2] Hence, to avoid transition errors within the decade Lippel suggests using logical detenting, *i.e.*, reading of the zone transitions in definite known sequence, and provision of a converter output only when the last relevant zone transition occurs. Because of the logical detent requirement Lippel needs as many as eight brushes per decimal decade. If a unit-distance Lippel code were used, the number of brushes required per decade could be reduced from eight to four or five. Lippel implies in his letter that unit distance Lippel codes are not known.

The code designated in Fig. 1 as $K=ABCD$ is one of the family of unit-distance Lippel codes. (Incidentally, K is of unit-distance but is not a reflected code.)

The family of unit-distance Lippel codes can be pictured on Veitch-Karnaugh Maps[3-5] as indicated in Fig. 2. O'Brien has recently studied reflected codes using Veitch-Karnaugh Maps.[6]

Any of the 96 subfamilies of codes pictured in Fig. 2 can have decimal 0 in any one of the ten utilized digit locations, and the progression 0-1-2 etc. can proceed in either direction along the trace on the map. Thus a total of $96\times10\times2$, or 1920, unit-distance Lippel codes exist. It can be shown by exhaustion of allowable transitional combinations that there are no other four-bit unit-distance Lippel decimal codes.

Logical detenting will still be required between decades, if conventional rather than reflected decimal output is desired, to insure that in a multiple-digit transition (*e.g.*, from 29 to 30) the high-order digit transition (2 to 3) is commutated first, but that the converter output does not reflect this change until the time that the lower-order digit transition (9 to 0) occurs. If reflected decimal output can be used, no logical detenting is needed, and only four brushes per decade are required.

Conversion of a unit-distance Lippel code to a standard weighted-count code is in general straightforward. For example, code $K=ABCD$ of Fig. 1 converts to the standard 5-2-2-1 code, shown as $K_1=A_1B_1C_1D_1$ in Fig. 1, as follows:

$$A_1 \leftrightarrow A$$

$$B_1 \leftrightarrow A\bar{B} \vee \bar{A}B$$

$$C_1 \leftrightarrow A\bar{C} \vee \bar{A}C$$

$$D_1 \leftrightarrow B\bar{C}\bar{D} \vee \bar{B}C\bar{D} \vee \bar{B}\bar{C}D \vee BCD$$

where $\leftrightarrow$ is "if and only if," the bar indicates "not," and V means "or, . . . or both." The expression for D_1 is the triple-exclusive-or, "any one or all three," which can be realized by a relay symmetrical circuit.

Conversion of the code $K=ABCD$ into the ordinary 8-4-2-1 code, shown in Fig. 1 as $K_2=A_2B_2C_2D_2$, is as follows:

$$A_2 \leftrightarrow A\bar{C}\bar{D}$$

$$B_2 \leftrightarrow B(C \vee D)$$

$$C_2 \leftrightarrow AD \vee \bar{B}C$$

$$D_2 \leftrightarrow A\bar{B} \vee (A \vee \bar{B})(C\bar{D} \vee \bar{C}D).$$

This conversion is less complex than conversion of the codes recommended by O'Brien.[6]

Further examination of unit-distance Lippel codes, using Veitch-Karnaugh Maps, might well reveal specific codes with simpler code-conversion rules; an exhaustive search has not yet been made.

$K = A\ B\ C\ D$
0 = 0 0 0 0
1 = 0 0 0 1
2 = 0 0 1 1
3 = 0 0 1 0
4 = 0 1 1 0
5 = 1 1 1 0
6 = 1 1 1 1
7 = 1 1 0 1
8 = 1 1 0 0
9 = 1 0 0 0

$K_1 = A_1\ B_1\ C_1\ D_1$
0 = 0 0 0 0
1 = 0 0 0 1
2 = 0 0 1 0
3 = 0 0 1 1
4 = 0 1 1 0
5 = 1 0 0 0
6 = 1 0 0 1
7 = 1 0 1 0
8 = 1 0 1 1
9 = 1 1 1 0

$K_2 = A_2\ B_2\ C_2\ D_2$
0 = 0 0 0 0
1 = 0 0 0 1
2 = 0 0 1 0
3 = 0 0 1 1
4 = 0 1 0 0
5 = 0 1 0 1
6 = 0 1 1 0
7 = 0 1 1 1
8 = 1 0 0 0
9 = 1 0 0 1

Fig. 1—A specific unit-distance Lippel code, K; the standard 5-2-2-1 code, K_1; and standard 8-4-2-1 code, K_2.

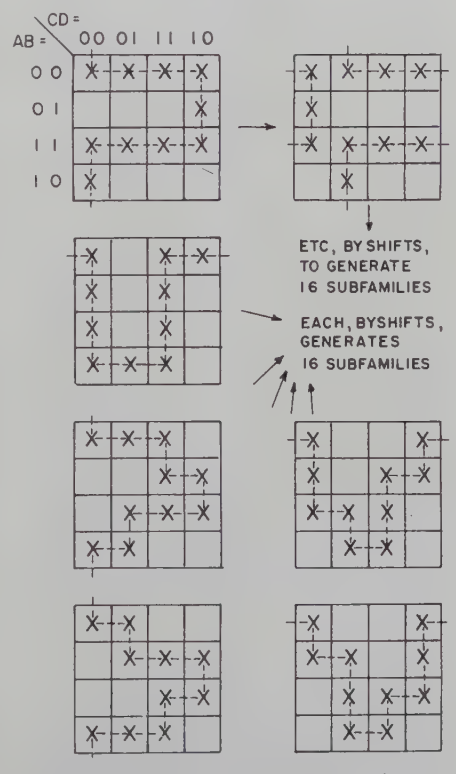


Fig. 2—Topology of unit-distance Lippel codes on Veitch-Karnaugh Maps.

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* Received by the PGEC, July 16, 1956. The work reported here was performed while the author was at Burroughs Research Center, Paoli, Pa.

[1] B. Lippel, "A decimal code for analog-to-digital conversion," IRE TRANS., vol. EC-4, pp. 158–159; December, 1955.

[2] In a code of "unit distance," code words representing consecutive numbers differ only in one digit position, and in that position the digits differ only by one. For example, the code "K" of Fig. 1 is of unit distance. A "reflected" or "cyclic" code is a special case of a unit-distance code, in which the sequence of code words follows a definite pattern with the mth digit from the right changing by one if and only if the $(m-1)$th digit is at its lowest or highest value, and with each digit changing successively from its lowest to highest value by unit steps, then back from highest to lowest value by unit steps. For example, the following numbers form a reflected decimal sequence: 01, 02, 03, 04, 05, 06, 07, 08, 09, 19, 18, 17, · · · , 12, 11, 10, 20, 21, 22, · · · . A recently published paper on reflected codes is I. Flores, "Reflected number systems," IRE TRANS. vol. EC-5, pp. 79–82; June, 1956.

[3] E. W. Veitch, "A chart method for simplifying truth functions," *Proc. ACM*, Pittsburgh Meeting, pp. 127–133, May 2–3, 1952.

[4] M. Karnaugh, "The map method for synthesis of combinational logic circuits," *Trans. AIEE, Commun. and Elec.*, vol. 72, pt. I, pp. 593–599; November, 1953.

[5] S. H. Caldwell, "The recognition and identification of symmetric switching functions," *Trans. AIEE, Commun. and Elec.*, vol. 73, pt. I, pp. 142–147; May, 1954.

[6] J. A. O'Brien, "Cyclic decimal codes for analog-to-digital converters," *Trans. AIEE, Commun. and Elec.*, vol. 75, pt. I, pp. 120–122; May, 1956.

An Improved Method for Williams Storage*

Two disadvantages of electrostatic storage (Williams' storage) are the relatively low read-around ratio and long access time while waiting for a regeneration cycle to be completed. Recent work on an electrostatic memory at Brookhaven National Laboratory in connection with a data handling project has suggested a mode of operation which greatly reduces these two disadvantages.

The normal electrostatic memory uses a double dot or dot-dash pattern, and gives output signals of the order of 1 millivolt. Past articles[1] have mentioned the dot-circle and dot-blur pattern, which give considerably larger signals. These have not been extensively used in the dot-circle case because of the extra complication of generating the circle, and in the dot-blur case because the blurring was accompanied by spurious deflection in the electron guns then available. Since this latter effect is not bad in the RCA 6571 tube, the dot-blur system is now just as simple to effect as the double-dot or dot-dash.

Three different considerations enter into the decision as to what beam current×time should be used.

1) The output signal increases as the charge (beam current×time) is increased when the same number is being continuously read and rewritten, as in reading or regenerating.

2) When a location is read the first time after a change from state previously held for a long time, the output signal increases as the writing charge increases.

3) The adjacent locations are disturbed more by reading and writing as the beam charge increases.

Thus the beam charge should be made: small to have the least effect on adjacent locations, large enough when reading to give an adequate output signal, large enough when writing to change the charge pattern to the new state.

For double-dot or dot-dash patterns the latter two beam charges are about the same. However, for the dot-blur system an adequate reading signal can be obtained when the reading charge is considerably smaller than the writing charge, *i.e.*, by only partially erasing the stored charge. This makes it possible to operate the memory in the following manner.

For reading (or regenerating), which means leaving the same information stored as previously existed, a low beam charge is used for the read and rewrite operation. If the cycle were interrupted after a read pulse and before the rewrite pulse, the information stored at that location would be only partially erased. Therefore, when that location was read again, the correct information would still be available, but at a somewhat lower level, perhaps 20 per cent smaller than normal. As long as it were properly regenerated on this second pass, it would not deteriorate to the point where it would be lost.

For writing, the beam charge is made large enough to establish a new charge pattern on the storage surface. It is possible to do this for all writing operations, or alternatively the location could be read and the larger writing beam charge used only when the stored information is to be changed from a 0 to a 1, or a 1 to a 0.

The fact that a regeneration cycle can be interrupted without loss of information means that when the computer calls for a number from the memory, the memory can immediately proceed to that storage location, read out the number, and then go back to the location it was regenerating and perform a complete regeneration. The same is true when the computer sends a number to the memory for storage. This means that the access time is only the time required to deflect to the correct location and read or write.

Since in any actual computer a storage location is read at least once to every write, and usually more, the read-around ratio will be somewhere between that for writing and reading (these are now different numbers since the beam charges are different for the two operations, possibly by a factor of the order of 5). A substantial increase in the operating read-around ratio can therefore be obtained.

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* Received by the PGEC, July 16, 1956.

[1] J. P. Eckert, Jr., H. Lukoff, and G. Smoliar, "A dynamically regenerated electrostatic storage system," PROC. IRE, vol. 38, pp. 498–510; May, 1950.

A Note on High-Speed Digital Multiplication*

In a recent paper Gilchrist, Pomerene, and Wong[1] showed how the carry logic of a digital computer could be arranged so as to make use of the theoretical result that the average carry sequence arising in the addition of two binary numbers is considerably less than the length of the numbers being added. In the concluding paragraph of this paper the authors made an estimate of the expected time for a multiplication using such circuitry. It is with reference to this estimate that this note is written.

Burks, Goldstine, and von Neumann[2] noted that if multiplication is carried out by successive additions it is sufficient to allow but a single carry at each intermediate stage and that a complete set of carries is needed at the end only. The question immediately arises as to whether this final set of carries obeys the same statistical properties as those formed in the addition of two random numbers. To verify that this is the case the numerical experiments described by Gilchrist, *et al.*,[2] were repeated with the modification that only one carry was allowed at each intermediate stage of the multiplication and the average length of the final complete carry determined. This was found to be 5.6 for the multiplication of two 40-digit numbers and the probability distribution of the maximum carry sequence was found to be the same as that for a simple addition given in Fig. 6 of Gilchrist, *et al.*[1]

The actual sequence of operations involved in performing such arithmetic is indicated in the logical diagram of Fig. 1

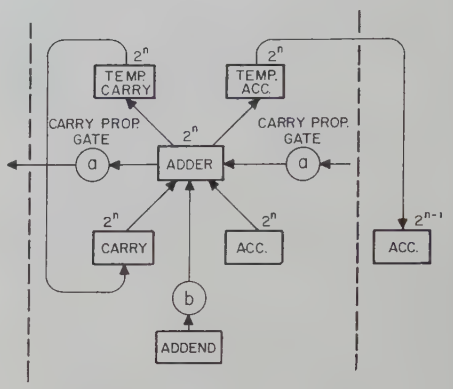

Fig. 1—Logical layout of the nth stage of the parallel arithmetic organ. The gates (a) are inhibited during all *interior* operations and enabled for the *final* operation. The gate (b) is enabled during all *interior* operations and inhibited for the *final* operation.

which shows an interior stage of the parallel arithmetic organ. At the beginning of a multiplication operation the inputs to the nth stage of the adder are the nth digits of the addend, the cleared accumulator and the carry storage register. The sum of these quantities is held in the temporary accumulator and the resulting carry is held in the temporary carry register.[3] The contents of the temporary carry and accumulator registers are then transferred into the permanent carry and accumulator registers. This operation is repeated for each interior step of the multiplication without, of course, clearing the addend and accumulator but with appropriate shifting of the accumulator. For the multiplication of two k digit positive numbers there are k such interior operations. As a final step the addend input is nullified and the carry propagation gates are enabled with the circuitry described in Gilchrist, *et al.*[1] A carry completion signal is then produced and the final sum placed in the accumulator.[4]

Utilizing the operation times given in Gilchrist, *et al.*,[1] and the fact that the average carry length in the last carry is 5.6, we obtain $41\times0.15+0.26=6.4$ μs as the average multiplication time exclusive of memory access. This compares with 10.2 μs in the case of no carry storage. The cost of this speedup is an additional register for carry storage and associated gating elements.

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* Received by the PGEC, July 16, 1956.

[1] B. Gilchrist, J. H. Pomerene, and S. Y. Wong, "Fast carry logic for digital computers," IRE TRANS., vol. EC-4, pp. 133–136; December, 1955.

[2] A. W. Burks, H. H. Goldstine, and J. von Neumann, "Preliminary discussion of the logical design of an electronic computing instrument," Institute for Advanced Study, Princeton, N. J., Part I, 2nd ed., 1947.

[3] These temporary storage registers may be actual toggles or delays.

[4] If the numbers are not both positive and only one set of complement gates is used, there are usually correction factors which have to be introduced in extra steps of the process. These should all be done prior to the long carry.

Fourier Analysis by Machine Methods*

Fourier analyses of experimental data are frequently carried out by either digital machines or analog equipments using a process closely paralleling the analytical expressions for the coefficients of the Fourier series.

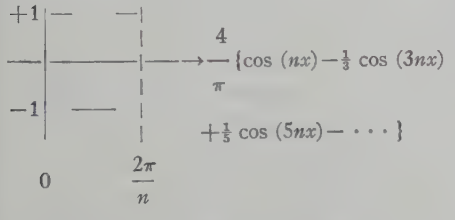
$$A_0 = \frac{1}{2\pi}\int_0^{2\pi} f(x)dx$$

$$A_n = \frac{1}{\pi}\int_0^{2\pi} f(x)\sin(nx)dx$$

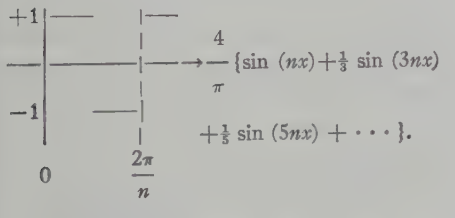
$$B_n = \frac{1}{\pi}\int_0^{2\pi} f(x)\cos(nx)dx.$$

In digital machines, a considerable amount of time is consumed in the computation of many values of sin (nx) or cos (nx), the many multiplications, and the numerical integration required for the determination of each component. In the analog realization, the multiplication of the two functions, $f(x)$ and, say, cos (nx), is generally quite cumbersome, expensive, and probably the largest source of error. The process described here overcomes most of the above difficulties by recognizing that multiplication by plus or minus unity is an extremely simple operation with either digital or analog equipment.

By analytical methods we find that the Fourier series for a unit square wave whose fundamental is cos (nx) is,



and for the square wave whose fundamental is sin (nx), we have,



* Received by the PGEC, July 16, 1956.

Now let us examine the values of the integrals of the product of $f(x)$ and a unit square wave such as one of those above. We have then,

$$\alpha_n = \frac{4}{\pi}\int_0^{2\pi} f(x)\{\sin(nx) + \tfrac{1}{3}\sin(3nx) + \tfrac{1}{5}\sin(5nx) + \cdots\}dx$$

and with termwise integration which is surely permissible if $f(x)$ is "band limited" as would be the case for experimental data:

$$\tfrac{1}{4}\alpha_n = A_n + \tfrac{1}{3}A_{3n} + \tfrac{1}{5}A_{5n} + \cdots$$

and similarly,

$$\tfrac{1}{4}\beta_n = B_n - \tfrac{1}{3}B_{3n} + \tfrac{1}{5}B_{5n} - \cdots.$$

Remembering that $f(x)$ is band limited (*i.e.*, has some highest order harmonic), we can see that the A_n and B_n are easily found from the α_n and β_n. For example, if the highest order harmonic in $f(x)$ were the 6th, the following tabulation would apply.

$$\tfrac{1}{4}\alpha_1 = A_1 + \tfrac{1}{3}A_3 + \tfrac{1}{5}A_5$$
$$\tfrac{1}{4}\alpha_2 = A_2 + \tfrac{1}{3}A_6$$
$$\tfrac{1}{4}\alpha_3 = A_3$$
$$\tfrac{1}{4}\alpha_4 = A_4$$
$$\tfrac{1}{4}\alpha_5 = A_5$$
$$\tfrac{1}{4}\alpha_6 = A_6$$

Thus we see that the highest order two thirds of the $\tfrac{1}{4}\alpha_n$ are equal to the A_n without further computation and the remaining A_n can be found by relatively simple computation.

To find the α_n and β_n with analog equipment we need only to generate $f(x)$ and simultaneously $-f(x)$; switch alternately from one to the other in accord with the appropriate square wave; and finally send this "switched" function to an integrator.

With the use of a digital computer, we can make a further simplification. For an example we will use α_2.

$$\alpha_2 = \int_0^{\pi/2} f(x)dx - \int_{\pi/2}^{\pi} f(x)dx + \int_{\pi}^{3\pi/2} f(x)dx - \int_{\frac{3\pi}{2}}^{2\pi} f(x)dx$$

$$= f^{-1}\left(\frac{\pi}{2}\right) - f^{-1}(0) - f^{-1}(\pi) + f^{-1}\left(\frac{\pi}{2}\right) + f^{-1}\left(\frac{3\pi}{2}\right) - f^{-1}(\pi)$$

$$- f^{-1}(2\pi) + f^{-1}\left(\frac{3\pi}{2}\right)$$

$$= 2f^{-1}\left(\frac{\pi}{2}\right) + 2f^{-1}\left(\frac{3\pi}{2}\right) - [f^{-1}(0) + 2f^{-1}(\pi) + f^{-1}(2\pi)].$$

Whence we see that the data describing $f(x)$ can first be integrated, say by Simpson's rule, forming

$$f^{-1}(x) = \int_0^x f(\tau)d\tau.$$

Since we no longer need $f(x)$, the new data describing $f^{-1}(x)$ may be stored in the same section of computer memory originally used for $f(x)$. The α_n and β_n are then formed simply from appropriate summing of values from the tabulated $f^{-1}(x)$. Furthermore, linear interpolation in the "table" of $f^{-1}(x)$ would correspond to parabolic interpolation in $f(x)$ if the integration were originally performed by Simpson's rule.

If one has reason to believe that a particular order of harmonic is the highest one present in $f(x)$, then this can be readily checked since all higher order α_n and β_n would also be zero.

Determination of the constant term, A_0, can be determined immediately from the full integral of $f(x)$.

The accuracy of this process is open to criticism particularly for the determination of the lowest order harmonics since these will have the combined errors of a large number of the α_n and β_n. Also, in the digital case, one might reasonably question the highest order harmonics if the data describing $f(x)$ provided only two or three points per cycle of the highest harmonic. However, the simplicity of the system makes it attractive.

It is interesting to note that a similar line of reasoning in which the square waves are replaced by their "derivatives" and associated with the corresponding termwise differentiated series leads to one of the graphical analysis methods which can be found in many of the textbooks.[1]

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[1] H. W. Reddick and F. H. Miller, "Advanced Mathematics for Engineers." John Wiley and Sons, New York, N. Y., 2nd ed., p. 202. 1947.

Symposium on the Impact of Computers on Science and Society*

This symposium was held at the 1956 National Convention of the Institute of Radio Engineers. It was organized by the IRE Professional Group on Electronic Computers and presented in the Starlight Roof Room of the Waldorf-Astoria on March 22, 1956. T. H. Bonn, Remington Rand Univac, Philadelphia, Pa., was chairman of the session.

The Editorial Board of IRE TRANSACTIONS ON ELECTRONIC COMPUTERS would welcome comments from readers on the publication policy of symposiums to be followed in the future. Comments may be addressed to the Editor.—*The Editor.*

CHAIRMAN BONN[1]: Gentlemen, welcome to the Symposium on the Impact of Computers on Science and Society.

Now, this is a very imposing title for a meeting. However, what we really mean is that this symposium gives engineers a chance to think of the broader implications of the digital and analog computers that we are working on.

Recent developments of digital and analog computers have had a profound effect on science and technology. Science has been given a new tool, the ability to perform calculations that were once considered impossibly complex and time-consuming.

In addition, the development of computers as a branch of technology has stimulated other new ideas which, in turn, are affecting other disciplines.

How are these facts shaping the course of scientific research and technological development? On what new goals are scientists focusing their attention, now that computers are available to them? These are a few of the questions which will be considered during this session. But we must do more than think of the effect of the computers on science.

We have been told by many that the development and widespread use of computers will bring about an economic revolution as great as or even greater in magnitude than the industrial revolution of the late 19th and early 20th centuries. The parallel has been drawn that, just as the industrial revolution was brought about by the use of machinery to perform many of man's routine physical tasks, so will computers perform the routine clerical and mathematical tasks. The combination of computers and machines, called "automation," permits a whole new group of tasks to be performed with a minimum of human intervention.

It's an acknowledged fact that the industrial revolution did have, and is continuing to have, a tremendous and not clearly understood effect on the lives of individuals and the problems of society. The effects on the individual and on society of the automation revolution may be even more profound, and the automation revolution will probably occur faster than the industrial revolution did.

We as engineers have been criticized in the past for failure to pay sufficient attention to the social and political implications of our work. We have been pictured as people who hew close to our scientific specialties, without devoting much time or thought to the general place of science and engineering in the world and the future of the things we are doing. I am very much afraid that to a certain extent this has been true. One of the reasons for this symposium today is to explore these social and political implications. Just as in other sessions of the 1956 IRE Convention, we are presenting papers and discussing technical subjects. But we are also going much deeper than that. We will consider the more profound and, perhaps, more widespread and lasting effects of our work. It is hoped that this session is a forerunner of similar sessions in future scientific meetings. We will try to lay the groundwork for some concrete problems which will act as a stimulus for future discussions throughout the fields of science.

Our first speaker today is Dr. Allen V. Astin, Director of the National Bureau of Standards.

Dr. Astin was born in Salt Lake City, Utah, in 1904. He received the B.S. degree from the University of Utah in 1925, and the M.S. and Ph.D. degrees in physics from New York University in 1926 and 1928, respectively.

In 1932 Dr. Astin became a staff member of the National Bureau of Standards, where he investigated problems of ignition, electronics, and electricity. He is credited with the discovery and development of improved methods of measuring dielectric constants and power factors of dielectric materials. He has also contributed to a better understanding of the nature of energy losses in air capacitors.

Dr. Astin has done pioneering work in the development of radio telemetering techniques and instruments as applied to meteorological problems of the earth's

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[1] The Chairman is grateful to R. J. Tuber, Technical Information Dept., Remington Rand Univac, Philadelphia, Pa., for assistance in preparing the stenotype record of the session for publication.

atmosphere and studies of cosmic rays. During the war Dr. Astin was chief of the Optical Fuse Section of the Bureau, and was assistant chief of the Ordnance Development Division. He became chief of the Division in 1948. As such, he played a major part in the development and evaluation of proximity fuses and in their introduction to service.

In 1950 Dr. Astin was appointed associate director of the National Bureau of Standards, in charge of the programs and activities of the Ordnance Development, Missile, Electricity and Electronics Divisions, and the Office of Basic Instrumentation. In 1952 he became director of the Bureau.

Dr. Astin has published many papers and holds several patents in his field. For his contributions and service, he has received many awards and honors, including the Presidential Certificate of Merit, 1948, and the Gold Medal Exceptional Service Award, Department of Commerce, 1952.

Dr. A. V. Astin: No one would deny, I think, that the American society of 1956 is changed from that of 1900. This change may be analyzed in many ways. The economist might describe it in terms of the gross national product. The demographer would use as his criteria population growth and the shift from rural to urban communities. And the electronic engineer, though he would rarely be called upon to do so, might describe this change in terms of the increased demand for his services and for the devices which he has helped to introduce to our economy.

Another way of analyzing this change is by looking at the relation of government to society. The role of government in the workings of our society has been significantly enlarged not only in size but in scope of responsibility. This may be readily appreciated when one considers the area of science. Since World War I, and to a greater degree during and since World War II, our government has become a major user, producer, purchaser, storer, supporter—or what have you—of the skills, data, devices, products, applications, and even personnel of science and technology.

Now this growth in government scientific activities is, I believe, characteristic of the growing responsibility of government to encourage technological progress in this country and to provide for the increasing scientific needs of a modern society. Furthermore, it is characteristic of the mounting and complex requirements associated with our national defense and welfare.

Such complexity carries with it a massive burden, and we must continually seek more effective techniques and devices to assist us in managing and arriving at best solutions to our complicated and varied problems. This brings me to the promise of the computer. It is a new tool with great and still unrealized potential. It is a magnificent tool which may greatly assist government in its scientific research activities and in many of its other operations. It is a tool whose flexibility, capacity, and speed make it capable of coping with some of the massive problems of science and the equally massive problems of government data processing.

I speak of the computer in terms of the future, in terms of its promise. All of you recognize, I am sure, that, despite the momentous advances that have been made in computer developments during the past five years, computer technology is still very young and the application of computational devices to science and data processing is still limited. This may be attributed to two reasons. First, there are still too few machines in existence—so few, in fact, that the impact of computer technology has only been felt in some isolated cases where urgency itself required that such devices be applied. Second, and even more important than this lack of computational devices is the critical shortage of trained personnel who can use, maintain, and build these devices. This is sufficiently serious so that the effective utilization of existing machines is impaired by this scarcity of trained manpower. These are the principal reasons which account for the fact that computational devices have not yet had a major impact on government. However, two other reasons should be mentioned. One is that present-day computers do have important limitations. There are large classes of scientific and data-processing problems which cannot be solved efficiently by these devices. The other is that the capabilities of existing machines are either underestimated or not fully appreciated so that it takes considerable urgency and justification before one considers converting standard procedures to automatic methods.

The state of computer technology, therefore, is somewhat ambivalent. On the one hand, insufficient use is being made of what we now have. On the other, active and continuous research and development is needed to provide machines which can cope with many existing and prospective problems. Thus, it would seem advisable to make increased use of present-day computers while continuing our efforts to improve the capabilities of these machines. What is needed also are scientists and engineers who will undertake systems and applications studies in order to broaden the use of computers for a greater variety of problems and operations and who will take advantage of and keep up with the latest developments in the field.

Let me now try to make these points more specific by telling you of our experience with SEAC, the National Bureau of Standards Electronic Automatic Computer. The SEAC began its operations in 1950. In terms of some recent developments, it may be considered an old lady, but it has been operating on a round-the-clock basis and has a considerable backlog of problems waiting to enter its input. The principal use of the machine is for mathematical problems arising in physics, chemistry, engineering, and to a lesser extent the biological sciences. Typical problems include the calculation of airflow and pressure distribution around an airplane wing or in a wind tunnel; the penetration of heat through fire-protection walls and the study of the conditions under

which spontaneous ignition occurs in stored materials; the penetration of nuclear particles and radiation through shielding materials; the design of optical lens systems; the computation of Loran navigation tables; the simulation of ground computers for guided missiles, and many, many more problems.

But despite this full-time utilization of SEAC and the growing accumulation of problems awaiting service by the machine, there are many problems which are beyond the capability of SEAC. Generally all problems arising in any branch of applied mathematics which are defined in terms of a partial differential equation in three independent variables are beyond the scope of SEAC. This is due either to the limited capacity of the machine or to its relatively slow speed. Furthermore, SEAC is not able to handle boundary-value problems in two independent variables for equations leading to more or less arbitrary matrices. And further, in some special cases, where the number of independent variables can be reduced at the start by employing some approximations, the SEAC may still be inadequate to the problem.

Recently, we made a survey of scientific problems which SEAC cannot efficiently handle. You may be interested in some of these and why SEAC cannot undertake them. There were problems in computing the probabilities of chemical transition which would require a machine-speed at least 50 times that of SEAC. There were problems in crystallography and optics which required speeds 100 times that of SEAC and much enlarged storage and memory capacities. Similarly there are problems in heat transfer, ferromagnetism, electron physics, radiation diffusion theory, experimental nuclear physics, molecular vibration, mechanics, and spectroscopy which call for higher speeds, increased storage capacity, and increased memory speed, and associated with these requirements, of course, there are needed refinements in input and output devices and techniques for increasing the life and reliability of components.

This is our current experience, but I think it may generally be applied to all computers now in existence and to the computer technology as a whole. We need bigger and better machines to approach many of the important problems of science.

The second major use to which the SEAC is put is for research and development associated with data-processing applications. Here our principal activity is related to the technical and advisory services provided by the National Bureau of Standards to other government agencies. Because of our early engineering experience connected with the development of SEAC and other government computers and because of our work in analyzing the requirements of certain government operations in terms of computational systems, we have become a scientific resource in this field available to other Government agencies which are contemplating the introduction of automatic techniques into their standard operations. The SEAC has been used, for example, to assist the Quartermaster Corps in handling procurement and bid evaluation problems, to aid the Navy in logistic and inventory problems, and to work out techniques for processing large masses of data, such as that encountered by the Census Bureau and the Federal Security Agency.

But even more than the use of the SEAC to assist in these special problems is the important analytical and engineering services which are provided by the National Bureau of Standards. This work is undertaken by our Data Processing Systems Division. The staff of this Division has been working with several Government agencies which are looking towards owning and operating their own automatic systems. Many of these agencies have approached the National Bureau of Standards for technical assistance. Typically, such agencies have asked for assistance in determining what areas in their activities are adaptable to these new electronic techniques and in detailed studies of equipment in terms of the requirements of their problems. Frequently, they have asked the Bureau if it would be possible to demonstrate feasibility by actual trial runs of representative sample data.

To undertake this work more efficiently, the National Bureau of Standards is now planning for the building of a new data processor, a pilot electronic device which will be suited to a wide variety of applications and which can simulate realistically the productive capabilities of a large number of different kinds of data-processing systems, in order that the equipment more suitable to the needs of an agency can be selected. In some cases, this new data processor will be used as an exploratory tool for investigating the novel performance characteristics demanded by special problems, and thus provide a realistic basis for specifications for equipment to be developed by commercial suppliers. This pilot device is being planned for adaptability so that it can handle data in the forms already utilized by agencies. We expect that this new device will not be placed in operation for about three years.

In the meantime, we are receiving more and more requests for information and assistance in this field. Let me summarize a few of these to show you the variety of problems which are now seeking electronic handling and the extent to which future government operations will be affected by advances in the computer and data-processing technology. In a project for the Bureau of Old Age and Survivors Insurance of the Social Security Administration, a National Bureau of Standards analysis team made a study of the feasibility of converting such operations to electronic data processing. This team concluded that the volume and complexities of the work of that agency were so large that automatic methods were urgent but that no system is yet available to facilitate that work effectively.

The Bureau, working with a committee from the Treasury, the General Accounting Office, and the Bureau of the Budget, recently completed an evaluation of proposals for equipment to perform the functions of

payment and reconciliation of all Government checks. A similar project is pending with respect to the issuance, clearance, and retirement of savings bonds. In the fields of logistics and supply, the National Bureau of Standards has been working with the Air Matériel Command of the United States Air Force and the Bureau of Supplies and Accounts of the Navy in evaluating the capabilities of high-speed computing devices which can be effectively used in logistics systems, inventory control, and accounting tasks. In these programs, some progress has been made, but we are far from maximizing the benefits which can be achieved with automatic electronic data processors. It is hoped that the Bureau's pilot device will help to accelerate the progress being made in this field. It is interesting to note, in connection with our work for the Air Matériel Command, that we have been conducting a training program for Air Force personnel, a training program in which relatively unsophisticated mathematicians are trained to program and use the computer for special purposes. This training program has proved quite successful and indicates that it is possible to increase substantially the number of people who would make use of the machine for nonmathematical purposes. I might mention also that similar work is being considered or undertaken for the Army and the Aviation Supply Office of the Navy.

Two other projects show further the range which might be expected of computational devices when applied to data processing. In one, the Bureau is engaged in evaluating the feasibility of mechanized patent searching and in determining the machine characteristics which will be needed. Our patent system is closely related to the industrial growth and prosperity of the United States. The present patent examiners are as dedicated and competent as their predecessors, but they face a task that is infinitely more complex than that of even a few decades back. The unprecedented pace of science and technology is producing new facts and inventions at a rate beyond the capacity for patent-claim handling procedures. In awareness of this problem, the Senate Appropriations Committee directed the Department of Commerce to make an investigation of the possibility of mechanizing patent search operations. A committee, headed by Dr. Vannevar Bush, was appointed. This committee concluded that if the patent system is to continue to make its contribution to our expanding economy, mechanization of the routine aspects of the patent search process is essential, and that the automatic data-processing art has reached a stage of development which makes feasible its application to this complex problem. Accordingly, the Patent Office and the National Bureau of Standards are cooperating in a joint program of research and development to adapt machine techniques to these Patent Office operations.

In another project, the National Bureau of Standards has been asked to study the feasibility of applying automatic data-processing techniques to certain problems of the Public Housing Administration. The Housing and Home Finance Agency is also burdened with massive information and data-handling procedures which cannot be managed adequately with present methods. The need for electronic techniques is urgent.

These projects are merely samples of the types of activities which are now looking toward automatic methods. In addition to these, we have received requests from more than 20 other government agencies for technical assistance of this type. The Bureau hopes to aid in conducting feasibility studies and in developing machine characteristics or in machine selection.

I have used the experience of the National Bureau of Standards primarily to indicate the growing interest and demand for data-processing machines and devices. But it must be understood that this demand is far from being fulfilled. There are still not enough machines or personnel to undertake all the known projects awaiting electronic methods. And what of the unknown projects? There are areas of government operations, I am sure, where there has been no thought given to automatic computational and control techniques. This may be due to any one or a combination of three reasons: 1) the failure to appreciate the efficiencies or economies which will be eventually provided by these electronic techniques; 2) the natural reticence of some to look to these radical devices for problem solution or data handling; 3) the lack of experts within given fields who can also apply themselves to the problem of converting standard operations to automatic methods.

So it is that we have made important strides in the application of computers to certain fields while other areas still remain untouched. And even in those areas where there are significant achievements, the impact is relatively small. It will grow more powerful, however, as time goes on. I think it is only a matter of time now before more and more agencies of the government seek the aid of the computer. As the number of papers, documents, invoices, records, and the like rises, as all this complexity increases in complexity, it is becoming more and more urgent that we look to these new techniques and devices to cope with this situation. I think we are only at the beginning of the age of the computer. It has already been demonstrated that the computer is a capable and most flexible instrument and that it can be put to a variety of uses and can be applied to a great diversity of problems and operations. As we advance in computer technology and as we learn to produce more efficient components and systems, the value of these machines will become even more apparent. I think it is in keeping with the phenomenal changes in our society that we continue to make advances in computer and data-processing research in order that we may be prepared for the changing requirements of the world of the future.

In conclusion, let me summarize what I believe to be the present state of the art of computer development. In the past ten years, there have been tremendous

achievements in this field. The value and the applicability of these machines have been fully demonstrated. Computers are now being incorporated into a number of scientific and operational situations. Despite this, however, the impact of the computer on our society and on government operations is still relatively small. The greatest impact is still to come. We still need to encourage a larger research and development effort in this field. And even more, we must educate and train a large body of scientists, engineers, and technicians to undertake this work. This will come, I feel certain, because the demand is growing and because more and more people are becoming aware of the importance of computer technology to the progress of science and society.

CHAIRMAN BONN: I think that some of you may have wondered why there are only four speakers' names in the program and we have seven people up here, excluding the Chairman. At the conclusion of the prepared talks, there will be a round-table panel discussion of some of the issues raised, and during the latter part of that discussion questions and comments will be solicited from the audience.

The three people who are sitting up here whose names do not appear on the program are Dr. Leon Cohen, Program Director for Mathematical Sciences of the National Science Foundation; Dr. John W. Mauchly, Director of Scientific Studies of Remington Rand Univac; and Dr. Arvid W. Jacobson, director of the Computation Laboratory, Wayne University.

Our second speaker today is Dr. Ralph E. Meagher.

Dr. Meagher was graduated from the University of Chicago with the B.S. degree in physics in 1938. The next year he received the M.S. degree, also in physics, from M.I.T.

During the war Dr. Meagher was a staff member and associate group leader at the M.I.T. Radiation Laboratory, where he worked on the design and development of Naval search radar. He concentrated on the design of indicator components and systems for radar. For this work Dr. Meagher was awarded the Presidential Certificate of Merit.

Dr. Meagher was a predoctoral National Research Fellow from 1945 to 1948, during which time he studied charged-particle scattering. He was awarded the Ph.D. degree from the University of Illinois in 1949.

After his graduate work Dr. Meagher became chief engineer of the group developing the ORDVAC and ILLIAC computers. He is now chief engineer of the Digital Computer Laboratory at the University of Illinois, and Research Professor of Physics.

Dr. Meagher is Editor of the IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, and is also a member of the National Science Foundation Advisory Panel on University Computing Facilities.

DR. R. E. MEAGHER: I think Dr. Astin has presented for you already what I consider to be a very good summary of the present status of computers. I'm going to take as my task a slightly different point of view and try to discuss it as I see it from a university man's viewpoint, and perhaps a midwestern university man's viewpoint.

I'm also going to take today's title a little bit literally —I hope not too literally—by discussing the aspects of computers in science first, and then say something about my own opinion concerning the society part of it. It is clear that a university man has a little bit more experience with the scientific part of the title than with the society part of it. I may, therefore, tend to emphasize the former, and the latter may be filled with my opinions rather than with my direct contact with society.

Well, I think it's very appropriate to consider these things now. It has been three or four or five years since the first round of experimental computers was finished, and it's also at a time when many commercial computers have found their way into use. Certainly we would all agree on some bases that the impact of these computers has been very great.

On the other hand, this greatness is very much affected by the particular field which is involved, and I think that we would all agree that the impact of computers on the physical sciences is the impact which is most completely felt at the present time. The reason for this is fairly obvious. The physical sciences are the sciences which first of all used computers, and which furnished practically all the impetus to build them.

As a result, today, for example, on the University of Illinois campus, where we have a large machine, much more time is devoted to physical science problems than to all others combined. I'll say a little more about other uses in a few minutes. The original impetus for the machine, its construction on our campus, and its use now, has been due to the physical sciences.

In order to say a little bit more about this, let me go back and point out that the physical sciences in general have had a long history in which instruments and tools have been particularly important. If we go back, for example, to the geiger counter, it was essentially this instrument which furnished a very large breakthrough in nuclear physics because of its ability to detect very low amounts of ionizing radiation; so it's nothing new, I think, to have one single instrument play a big role in the physical sciences.

Since the last war there have been two instruments which have had a big effect on the physical sciences. One of these is the pile, as a neutron source. The other instrument with a big effect is the electronic computer.

In the physical sciences, the pile has its most direct application, perhaps, in physics, and recently some application in certain engineering fields. I think the computer has had a bigger effect on physics even than the pile. What's more important is that the computer isn't limited quite as much to physics as the pile, although its use has been mainly there so far. It's a general instrument which can be used in many other fields.

In view of Dr. Astin's examples of some important problems in physics, I will take the time to mention only

one of them which is of current interest on the campus at the University of Illinois.

Physicists nowadays are engaged in an effort to get higher-energy particles—their Cosmotron and Bevatron are examples of this.

At Illinois, a group of midwestern scientists has been using our computer, the ILLIAC, for designing a new machine in the 30-billion-electron-volt range. This problem has two important aspects which I want to mention.

First of all, an accelerating machine can be designed by building a model or by solving the differential equations for the motion of the accelerated particles. One of these procedures needs to be followed because the path of a particle is not a perfect circle and the extent of the deviation from a perfect circle needs to be known since it has a great effect on the size and cost of a machine. Building a model is costly for a large machine. The differential equations of the particle motion can be solved on a digital machine even with the alternating magnetic fields proposed for the new accelerators. The accelerating machine can then be designed and redesigned by solving the differential equations, and then altering the constants and resolving them. When the latter procedure is used, the great cost of a model is eliminated. Indeed, the equations can be solved so readily on a digital computer that many more cases can be considered than would be possible with a physical model. Incidentally, when the ILLIAC is used it takes the particle about one minute to go around the hypothetical circle once, using the constants for a typical 30-BEV accelerating machine. The use of a computing machine has greatly reduced the cost of the design of an accelerating machine (or has greatly extended the particle energy available for any given cost) because it can produce a better design than would be possible with models.

Now the way I have stated the accelerator problem it may sound as though it is a straightforward extension of hand computation techniques and basically this is so. However, the ability to change with ease the constants in the equations means that the constants can be altered by small or large amounts and the results of this observed. This is just the way an experiment is carried out with apparatus. Thus the second aspect which I wanted to indicate by this accelerator problem is that experimental work in a rather literal sense can be carried out with an electronic computer.

In a related way but on other problems it can be said that theoretical physicists (who traditionally do little experimental work) are doing experimental work!

I think the impact of the computer on the physical sciences has been very great. Undoubtedly this will continue, and it's probably from these groups that requests for new and bigger computing instruments will continue to come.

The other sciences, the nonphysical sciences, such as social science, psychology, and so forth, have so far used machines to a comparatively small extent. This is quite obviously because people in the social sciences have less mathematical training. Even so, big inroads in this are being made, and on my own campus, at least, something like 10 per cent of the computing machine time is devoted to social-science problems. Although this is small percentage wise, it accounts for a large number of problems. Their problems are usually simpler than the problems of the physical sciences and they are shorter.

There remains an educational problem of acquainting the people in the nonphysical sciences with the importance of computers. This will take time as well as additional mathematical training over and above that which many social scientists have considered adequate.

Education, therefore, plays an important role in the future importance of computers in the social sciences much more than in the physical sciences. Education is also the important part which remains to be carried out in other nonscience fields and the need for it certainly represents one of the reasons why the use of computers may be held back in the near future.

As I have said, on my university campus, practically all of the impetus for the computer has come from the physical sciences, with no participation from business or commerce areas. This is a mistake, I think, and it can only be rectified by additional education.

I have the opinion that the social sciences will use computers much more in the near future.

Let me turn my attention now to the "society" part of our symposium title about which I am less qualified to speak. My opinion is that the impact of computers on society is relatively small. Even though commercial machines are finding their way into many companies and many industrial uses, it's clear that at least in the beginning this use will be confined to rather straightforward business problems in which the over-all analysis of the problem has already been made in principle, and where it's pretty much a matter of coding in order to get it onto the machine.

I am oversimplifying the problem a little by saying this, but I wanted to do this purposely, because I think that as the business machines are being introduced now, their field will be rather restricted only to what I shall call the arithmetic kind of problems which occur in industrial and business computation. Probably the rate at which new computers are being introduced will barely keep up with a growing need for business arithmetic.

Somehow, there's a very big field left open here in which practically nothing has been done. I like to think about it as a field in which the term "operations research" should apply, but this term isn't very well defined, and some of you may wish to call the field "automation." Whatever it may be called, I think that a great deal of work remains to be done in the analysis and programming of problems which will affect not just the business applications—that is, the computations concerning money—but those areas which affect operations both in industry and in government.

At the present time I think that this may be very slow in coming. I feel that the computer engineers have a

tendency to feel now that the main job in computer design work has been completed, that the basic ideas are known, and perhaps this is so. Many of them feel that what's left is to transistorize the existing models.

Certainly this will be an important step, but I don't think that it will be enough. Computer engineers should have a very far-reaching attitude toward integrating computers into more aspects of our industrial and nonscience fields. This could come about by considering much more integrated systems than have formerly been explored.

In the past, the computer has been a thing which sits in a room by itself, to which one walks with a set of cards or tapes. Instead of this I think that the computer should be integrated into an industrial operation so that communication between the computer and the individual will not have to be as direct as it is now.

I haven't seen any new ways of doing this, but I think this is one of the fields in which computer designers should spend a large amount of time in the near future.

Let me summarize, then, in the next couple of minutes, so that I will finish on time, the things which I feel about the impact of computers on science and society. I think the impact of computers in the physical sciences has already been great, although it certainly will be much greater in times to come.

I think the impact of computers on the social sciences is small, but increasing rapidly.

I think the impact of computers on nonscience fields is relatively quite small, even though in absolute value it may be large.

If we are to go ahead, I think we should furnish bigger and faster computers for the physical scientists who are ready and willing to make use of them directly.

I think that commercial computers should be slanted more toward the over-all problems, even the over-all special-purpose problems which do not require human insertion of all data through one or two input mediums. An operational research approach should be used in deciding on the system as well as in its eventual use in industrial applications. Thank you.

CHAIRMAN BONN: Our next speaker is Dr. David Sayre.

Dr. Sayre received the B.S. degree in physics from Yale University in 1943. From then until 1946 he was a staff member of the M.I.T. Radiation Laboratory. From 1947 to 1949 he was research associate on Computer Design at the Auburn Research Foundation.

Dr. Sayre was awarded the degree of Ph.D. in chemical crystallography at Oxford University in 1951. During that year he was scientific consultant for the London ONR.

Dr. Sayre was an associate at the Johnson Foundation for Medical Physics at the University of Pennsylvania until 1954, when he joined the Programming Research Group at IBM Data Processing Center in New York.

He is now serving there as senior mathematician and assistant group manager.

DR. DAVID SAYRE: When Mr. Bonn invited me to talk at this symposium, he asked me to say something about the impact of computers in the field of biology, and I shall begin by doing so. The impact of computers on biology, so far, has been rather small. I think we may search for a reason for this, and formulate it as follows: that in comparison with those of the physical sciences, the procedures that biologists have arrived at are inexact and incompletely formulated. It's very difficult with our present techniques to carry out such a procedure; I shall say no more about this phrase "inexact procedures" at the moment, but I will return to it later on.

There are, however, a number of fields in biology in which profitable use could be made even now of our present-day machines. I'll mention one example. Some of the most ambitious of the neurophysiologists have begun a most difficult project of exploring, with 2- and 3-dimensional arrays of probes, the electrical activity in specific regions of the brain. The task of reducing this very large amount of information about the electrical potential at so many points in the cortex to a form in which a correlation becomes possible with the stimuli reaching the brain through the sense receptors is surely a data-processing problem in which our machines can be useful.

You have heard that I took my degree in a science called chemical crystallography. That is one name for what is more commonly called X ray crystal-structure analysis, a technique for producing a photograph of a molecule with resolution enough to show clearly the position of every atom in the molecule.

Crystallography, of all our structure-determining methods, gives the greatest promise of solving the structure of a protein molecule, a problem of the highest importance in biology. As Dr. Astin mentioned, the calculations involved in X ray analysis are very cumbersome, and it is becoming increasingly common to carry them out on high-speed machines.

I have been working during the last year at IBM on a set of programs for doing X ray crystal-structure analysis with the aim of making it possible for one to arrive in the morning with one's X ray experimental data about a complex molecule, and to leave in the afternoon with the complete structure worked out.

Even if it should be another ten or twenty years before techniques of this kind can handle structures as complicated as proteins, I believe that in a much shorter time they will be capable of handling the structures of moderate complexity that the chemical industry is usually interested in. If this is so, a minor revolution will occur in the methods of industrial chemistry, and classical organic chemical analysis will be largely supplanted by the X ray method.

As a final example of the effect of computer technique on biology, I should like to point out that computing experts may before long begin to make significant direct contributions to our understanding of mental activity.

We at IBM—and we are by no means alone in this endeavor—are beginning to take the first groping steps toward endowing machines with something that we may call intelligence, and those of us who are engaged in this kind of thinking (perhaps because we are not trained psychologists) find it very easy to convince ourselves that we are in fact doing quite good psychological studies. As this field develops it is quite possible that computer designers and programmers will be contributing papers to the psychological journals.

Let us turn now to the impact of computers on society. I shall take as my starting point my belief that our technical ability will prove equal to any demands that our society as a whole is likely to lay upon us; that whatever ceiling is placed upon the role of computers in the affairs of mankind will be dictated not by technical considerations but rather through economic considerations, possibly through the difficulty of providing the human resources to carry out the tasks necessary to realize such goals, or, in the broadest sense, through a reluctance on the part of mankind in general to elevate machines to a position of such importance in our affairs.

If this is so, then we as engineers and computer technicians are, in a sense, absolved from the decision as to how far computer technology shall go. We naturally, as people, must take our responsibilities in these decisions, but we are not going to provide them as unmistakably as if we were to say, "We can't do it."

Therefore, we are free to talk now not about our societal responsibilities, but to talk about what we, as computer people, should do if society asks us to go ahead.

In attempting an answer to this question, I shall ally myself with Dr. Meagher in the following sense: so far, we have all, I think, tended to think of computers as essentially mathematical computing devices. In my opinion, this is only the beginning. It's a rather young attitude on our part.

The real importance of machines lies in their capacity as general logical devices. It's very easily understandable why, during these first ten years of computer technology, we have thought of them generally as calculating devices, but it is equally clear, I think, that the really big problems, the problems which can greatly affect scheduling of production, with the planning and control of traffic in an airline or railway system, or in general with the efficient conduct of any complex activity, will require on our part a rather different technique of machine use than we have yet developed. For these problems are problems for which no exact procedure has been evolved. Nobody knows how most efficiently to handle traffic in an airline system; Dr. Meagher undoubtedly had such problems in mind when he referred to the importance of operational research.

It follows, I think, that the next major challenge to computer technologists will be to learn how to get the machine to do part of the work of formulating procedures. I should define a first goal as follows: that we learn how to cause a machine, which has been given a fairly exact procedure, itself to amplify and correct it, constantly producing better and better procedures.

Now, we have begun this kind of thinking. So, I am sure, has every other computer manufacturer and many universities.

Already an important result is at hand—the development of automatic coding techniques, such as our own FORTRAN, which enable the programmer to state his procedure to the machine in a language hardly different from the language he would use in discussing it with another person. The machine is equipped with a program capable of translating this language into the machine's own language—that is to say, into a procedure ready for running on the machine. Automatic coding techniques will unquestionably do much to simplify the problem of communication with machines and therefore to relieve the shortage of programmers. But they also constitute a first step toward the achieving of the goal of automatic procedure development; it is through them that the impact of computers on us all will ultimately be expressed.

CHAIRMAN BONN: I'm sure that very few of us here were aware of the uses that the biologists are putting computers to, and I'm very grateful to you for telling us of them.

We have now reached approximately the half-way point in our symposium, and I would suggest that it's time for a brief intermission. I would suggest ten minutes. According to my watch it's now ten minutes after eleven. We will reconvene here at twenty minutes after eleven to hear Dr. Forrester, our fourth distinguished speaker. Thank you.

(The meeting was recessed about ten minutes.)

CHAIRMAN BONN: I have been asked by a member of the audience whether the proceedings of this session will be published. We have a stenotype record of the session being taken, and in addition we have Richard Tuber of the Technical Information Department of Remington Rand as a reporter here, and with the cooperation of the speakers and the panel members and everybody else involved we will try our hardest to get the proceedings published in the TRANSACTIONS OF THE PROFESSIONAL GROUP ON ELECTRONIC COMPUTERS.

I don't think we have enough time to meet the deadline on the CONVENTION RECORD, which is very, very soon.

Our last speaker today is Dr. Jay W. Forrester. Dr. Forrester was graduated with the B.S. degree in electrical engineering from the University of Nebraska, in 1939. He received the M.S. degree from Massachusetts Institute of Technology in 1945, and in 1954 he was awarded the honorary degree of Doctor of Engineering from the University of Nebraska.

Dr. Forrester was one of the cofounders of the Servomechanisms Laboratory at M.I.T. in 1941. From then until 1945 he participated in the development of electronic and hydraulic control systems for the direction

of gun batteries and stabilization of shipboard radar antennas.

Since 1945 Dr. Forrester has been in charge of Project Whirlwind for the development and study of the applications for high-speed electronic digital computation. He worked on the initial development of the random-access magnetic-matrix memory, now beginning to replace other types of high-speed internal memories in digital data-processing systems.

Dr. Forrester has been director of the M.I.T. Digital Computer Laboratory since its formation, and is also head of the computer division of the Lincoln Laboratory at M.I.T.

Dr. Jay W. Forrester: Thank you very much. I think I will try to make a few disconnected comments this morning of a rather controversial nature, in the hope that we can get our discussion panel to rise up in protest and make an interesting session for the rest of the morning.

Many discussions in the computer field these days revolve around the shortage of engineers and scientists and the shortage of people to work with computers. I think the shortage goes a lot farther than just the engineering and scientific personnel. I want to say more about that later, but maybe a few words might be in order suggesting that we keep our perspective on the matter of an engineering and scientific personnel shortage.

We see in the newspapers all the time references to the serious shortage of engineering personnel. What do we mean by this shortage? It's an absolute shortage, not a relative shortage. It's a shortage in the sense that we would like to have more engineering personnel, but it's not a shortage in the ordinary economic sense, apparently.

If you have a real shortage of copper, a lot of things happen. The price of copper goes up, and people go about getting more copper, and they start more copper mines.

But look at the engineering situation: none of these things have happened. The price hasn't gone up and little is being done about increasing the supply.

Some of you laughed when I said that the price hasn't gone up. It's generally assumed that it has, but look at what's happened in the last 15 years. In the last 15 years the consumer retail and wholesale price index has increased by a factor of 2. Engineering salaries have gone up by a factor of 2.2. (This is one-eighth more than the price index.) Construction workers' wages have gone up by 2.7, manufacturing workers' wages by 2.8. Some of the commodities have increased a great deal more than that.

So, in the economic sense there has been no reflection of a shortage of engineering personnel.

Neither have we done a great deal about going back to the source of the shortage and doing anything about it. As one economist told me, there is a shortage of engineers just as there is a shortage of Cadillacs. You would like to have five Cadillacs, but that doesn't prove that there is a shortage of Cadillacs.

Yesterday morning at the Engineering Management Section there was a discussion pointing out a concerted effort in the Los Angeles area to increase engineering enrollments. The engineering societies there have succeeded in doubling the engineering enrollment in the colleges. While this is a commendable effort, it could be carried too far, obviously, even as far as unbalancing the rest of our society.

The point is that there is a shortage of good people in all kinds of enterprises. I was talking to a vice-president in charge of sales here a few months ago, and you would have thought he was an engineering vice-president talking. He pointed out the shortage of good salesmen, how people weren't available to fill sales positions, and how the high schools ought to be interesting more people in the promising future of being good salesmen. This is happening in every field at the present time. We're in a competitive situation that hasn't yet worked out to a steady-state solution. We need to keep in mind other forces around us, what other people are doing, and what their problems are, in order to plot our own course.

While I'm on this matter of supply and demand, I have made a note on one of the characteristics of the computer field—the tendency to overload the facilities we have available regardless of their capacity. It matters not whether the facility be a clerical organization or a computer of 1000 times the capacity.

Therefore, I would like to raise a couple of questions that can be discussed later. Dr. Astin pointed out the serious need in the Patent Office for automatic handling of patent applications. It might be worth reflecting what would happen if we had more automatic equipment in the Patent Office. Would it really be a good thing?

I don't propose to answer the question of whether or not it's a good thing, but what happens if we have automatic equipment? We will get more patents and more patent applications. There is considerable doubt as to the value of most present applications. Better patent machinery will mean more patent applications. If we make it possible to handle ten times more patent applications, what have we really accomplished? Companies can trade patent licenses on the basis of 20-foot stacks of documents instead of 2-foot stacks, but the relative situation won't be changed.

The point I'm making is that the number of patents at the present time may be limited by the difficulty of getting a patent, and not by any inventiveness limitation in the population. So, whatever facilities we have may very well be loaded to the point where the unsatisfactory state of affairs acts to limit new applications.

Of course, if I wanted to be a real cynic, I could make the same comment about machine translation of languages. Very few of us have an opportunity to read available material in the languages that we know.

However, ignoring the comments that I have just made, let's look at what the computer field needs. It needs not only engineers, but it needs an informed public. It needs people in many fields, many walks of life, who know something about computers and how computers will relate to their own interests.

Those of you who attended the Joint Computer Conference in Boston, which was devoted to business applications, will recall the difficulties of the banks and oil companies who are attempting to use computers for customer accounting. Most of their really serious problems revolve around the acceptance of the new methods by the public, what changing their methods will do to their competitive situations, and feeling that the public may not understand what they are doing. I think this is one of the very serious problems that we face.

At the other end of the scale, we need a better understanding of the potentialities of these machines amongst executives in the business world. This has been touched on by the previous speakers. As a theoretical foundation for computer applications, there is a great deal that can be done in the theory of inventory control, the dynamic flow of information and materials, the welding of the computer art with the groundwork that's been laid in feed-back theory and servomechanisms in the last 15 years, and in wrapping these up in one package through the use of computers as simulators in the same way they have been used to test engineering designs in the last few years. The use of digital computers as simulators of physical equipment can be carried over directly into simulation of money and material flow with respect to the individual industrial company, and also with respect to the economic system on a larger scale. I think here lies a very great challenge, an opportunity which has been opened up by the computer. The problems themselves can be formulated but are too complicated to be handled without the computing capacity made available by the new machines.

But when we get into industrial applications of that kind, people in inventory, warehousing, accounting, and throughout our industrial companies need to have an understanding of the new methods. One can't do these things without a great deal of "grass roots" support from within the company. A lot of people have tried to revolutionize operations on too short a time scale, trying to do it in two, three or four years, and it's a frustrating effort when they find that their associates don't understand, and, in fact, don't care.

Now, if we want to bring in the kinds of people whose lives will be touched by the computer field, I think we can find these people, these future engineers, computer operators, nonprofessional workers and business people only in our high schools.

Computers so far have been taught in graduate schools. That's much too late a time to introduce this universal field into our educational processes. It's important that college undergraduates—probably even in the freshman year—be introduced to the preciseness of digital computers as an exercise in preparing precise, unambiguous descriptions. Some exposure to computer programming has a universal value, even to those who never use it, and is well within the grasp of the undergraduate, or even of the high school student. It's a misconception, I think, to believe that digital computers can be understood only by engineers and mathematicians.

We have been very successful in our own work in bringing in people from accounting. Actuaries, and even music majors, have done outstandingly good work in computer programming.

In the next two decades, automation in the factory and electronic information processing in the office will free many men and women from their present types of work. It will be necessary to attract many of these into the design, construction, and management of electronic information-handling systems in the various fields in which these machines will be employed—the scientific fields, the business applications, and the control applications.

We must reach, then, into the high schools and to the public with the message that these new developments are understaffed. They are crying for more people, rather than being a bugaboo that will create unemployment. You will find a real fear of these new developments on the part of many people, an unjustified fear which I think needs to be counteracted.

This idea of carrying the engineering story to the high school level is now being given serious thought by a number of organizations. I will read to you one news clipping:

> "An experiment aimed at increasing the number of adequately trained high school mathematics teachers has been launched by Arthur D. Little, research consultants, and the Lexington, Massachusetts, School Committee. The Lexington plan is a program to attract young teachers by providing them with an income closer to that provided for technically trained young people in industry by giving them an opportunity to work directly in industrial research as an adjunct to their teaching assignments.
>
> "Under this plan two new graduates with degrees in chemistry, physics, biology, or mathematics will be hired for three years to fill one science teacher's position in the Lexington High School. One will teach the first half of the school year, and the alternate will teach during the second half. Both will work at Arthur D. Little's when not teaching.
>
> "During the teaching period each individual's income will be that of a Lexington High School teacher with similar qualifications. Arthur D. Little will pay its regular rates while the teacher is with the Company. Thus the total income for each will be considerably greater than either could earn by teaching on a full-time basis alone."

Another approach to this same problem was sug-

gested recently by David Sarnoff, Chairman of the Board of the Radio Corporation of America, in the speech that he gave before the National Security Industrial Association on January 26. General Sarnoff said in one part of his talk:

> "I propose the establishment of a national educational reserve comprising qualified teachers in mathematics, physics, chemistry, engineering, and related subjects to be brought from the technological ranks of industry. I have in mind the release—and with full pay—for at least a year of a reasonable number of men and women for teaching assignments in their local schools. This unique reserve could also mobilize those who have reached the retirement age in the military service and in industry, but whose knowledge and experience would make them inspiring teachers."

Your Chairman asked me to review and repeat some of the suggestions which I made at the Joint Computer Conference in Boston last November. At that time I made a proposal that we arrange to have a team of full-time men, perhaps five or six, one donated by each of the several large industrial concerns in this field, who would work together, not as ordinary professional committee members meeting occasionally, but as a full-time working group with no other goals for a period of a year, and that they do this under the auspices of the Joint Computer Conference, which is sponsored by the IRE, the AIEE, and the Association for Computing Machinery.

This proposal has now been approved by the three societies, and the Joint Computer Committee in undertaking to establish the group.

Such a working group could do many helpful things. They could provide sound and creative information for the kind of people who make toy kits for the consumer market. Another approach is to make arrangements with a good author who knows the high school audience level and help him write on computers and automation describing the kind of work that people will do with these machines and the impact that they will have on society—in other words to answer the questions that the high school students are now asking.

Also, such a working group could encourage exhibits for our science musems. I am very sure that the science museums would enthusiastically participate if they had a little encouragement and some sources of information. Particularly, the group should plan to help the high school science teachers in various ways, such as narrated film strips, supplies for laboratory work, and various reading material. Do-it-yourself instructions would be important for showing how to use old radio tubes and relays in simple computer-type devices. Most of the industrial companies have very good booklets which are related to the subject we are discussing, but they aren't generally known and available. Such a group could help distribute the available information.

In Boston I discussed one way to finance such an educational program. There may be others, but a straightforward approach would be to consider such a program as a normal and an important part of doing business in a new field. There are about 30,000 high schools and they have in them about 7 million students. The companies which are predominantly in the electronic data field have combined yearly sales of about $1,200,000,000.

I would suggest that these companies might well afford to take 1/10 of 1 per cent of sales for a joint industry educational program at the high-school level. This makes a yearly budget of $1,200,000, which is $40 apiece for each high school in this country. Compared with the 2 or 3 or 5 per cent or higher that each of these companies is spending on physical research to develop equipment to be sold to the bewildered public, I think it's a fairly small price.

Thirty dollars to $50 per high school per year should carry a very successful program. This kind of money is relatively small, compared to what we spend on research, compared to other public relations expenses, and, indeed, compared to advertising costs to try to attract engineers from the end of an educational pipe line which we are making an insufficient effort to fill at its source.

CHAIRMAN BONN: Thank you very much, Dr. Forrester. I'm sure that there will be many comments on your proposal.

Before starting the panel discussion, I would like the various members of the group up here who have not yet spoken to identify themselves by rising as I call their names. We have Dr. John Mauchly, Director of Scientific Studies at Remington Rand Univac; Dr. Leon Cohen, Program Director for Mathematical Sciences with the National Science Foundation; and Dr. Arvid W. Jacobson, Director of the Computation Laboratory, Wayne University.

Now, one of the things that has been stressed by each speaker is the need for trained people in the computer field, and Dr. Cohen in connection with his duties in the National Science Foundation would like to tell us very briefly what the National Science Foundation is doing along these lines. Dr. Cohen:

DR. LEON COHEN: Perhaps before I indicate what has been going on in the thinking of the National Science Foundation with regard to the matter of computation, I might make a comment or two on some of the questions which have been raised, because they will set the stage for some of the directions in which we are trying to move.

The question of biological applications was raised, and I asked Dr. Sayre what he thought of a comment which I heard from the professor of medicine on the Johns Hopkins faculty a couple of years ago, that went as follows:

> "Daily through the pathology laboratories of the hospitals in the United States there passes an enormous amount of information, the results of the

analyses made there. Question: What happens to these data? How are they processed? How are conclusions drawn as to the problems of health which are involved here?"

Apparently this might be a subject for consideration by computer people.

With regard to sociology and economics, an interesting phenomenon has turned up in the last couple of years. A curriculum for first-year mathematics for students intending to study sociology, economics, and the like, has been recommended by the Social Science Research Council. In the curriculum they have emphasized algebra of sets and linear transformation—matrix theory. When you consider that the engineers consider this a very sound basis for the beginning of their education, the gap between the social sciences and the engineers may not be as large in the future even technically as it has been in the past.

One could go on this way, but I'll switch this to another point of view, taking account of the question of demand for personnel which Dr. Forrester raised. In 1953 a gentleman connected with one of the large computing-equipment companies stated that on the basis of their equipment then in the field there were needed 1500 mathematicians. About a month ago a gentleman from the same company spoke to me and said they now need 7500.

I was interested in this not only because of the numerical rate of growth. I said, "How are these people to be distributed with regard to depth of mathematical insight? How many will you need, say, at the Ph.D. level, the M.A. level, and the A.B. level?" This type of information was not forthcoming.

It's clear with this growth in the demand for numbers that if some information is not available as to the depth of training, it will be very hard to find out what the time scale is. It takes considerably longer to make one kind of these people than it does to make another.

So, then, you have the range of possibilities facing people who are interested in computer techniques. You have the demand of a whole spectrum of knowledge for preparation for this, and you ask: what are the devices by which the appropriate people can be produced?

Well, I have heard some comments on them, and they seem to run like this: in the first place, appropriate people will need the right kind of mathematical training. I won't go into the question of what is the right kind. This is the subject of much debate.

They will also need a feeling for the capabilities of computing equipment, and furthermore they will need something which I tried to formulate in a slight variant of the current psychiatric slang—namely, they will need a freedom from intellectual inhibitions, instead of emotional inhibitions. That is, if a problem comes along which doesn't get into the classical set of mathematical models, they must not just turn up their noses at it.

I suppose to get people of this sort probably the right place to look is in the universities and in the leading technological institutes, because only in such an environment can you have the variety of intellectual tendencies which must exist, the proper inhomogeneous mixture to constitute the proper background.

Therefore, since you want this inhomogeneity, you would like to have a computing laboratory, if it is to exist in such a place, not be in the special departments or divisions of the institution which has at the moment maximum need.

Now, this is not an argument to say that the department of physics should not have the most magnificent, complete equipment available, because they have enormous problems. They should have it, but it will not meet the need for this inhomogeneity which the future faces. Therefore I suggest that a computing laboratory for a university should play the role of the general university library. A departmental library is a magnificent tool, but it is occupied full-time, and should be, by that department or that division; whereas if what the speakers have in mind is an accurate indication of the future, there must be access from every kind of intellectual curiosity to the computing center.

Well, then, one tries to do this sort of thing. The next problem that comes up, I suppose, is this: that the facility which is to be provided should not, at least at the moment, be so large as to overtax, to the point of presenting an insurmountable obstacle, the financial resources available or the staff resources available. On the other hand, it should be large enough so that significant problems involving automatic computation can be handled, in order that an appropriate research and education program involving both the faculty and the students can be gotten under way.

These are the ideas which have emerged during the last two years at the National Science Foundation with the advice of a panel chaired by John von Neumann, containing a group of people representing physics, chemistry, mathematics, engineering, and several other disciplines. There are hopes that within a reasonable time now some tangible results may come out of this thinking, and if it were two weeks later I might be able to make more definite statements, but at the moment I I can't. Thank you.

CHAIRMAN BONN: Thank you very much, Dr. Cohen. A. W. Jacobson, would you care to comment on some of the experiences of Wayne University?

DR. A. W. JACOBSON: First of all I wish to make a few remarks concerning the educational problems with which we are confronted as a consequence of the advent of the electronic computer.

I feel that the computer technology is essentially a continuation—in fact an accelerated continuation—of the processes generally described by the term "industrial revolution." I do not think it is necessary to discuss this in further detail; it has already been done at this meeting. I do, however, wish to emphasize the significance of the computer development especially as it ap-

plies to the social sciences, information processing, and automatic control. These features are additional and in some ways of higher order than those processes which characterized the "industrial revolution."

The ability to have more information on large operations and to know the current trends are of real significance in terms of social control. This newly acquired power has an interesting significance in the philosophy of history. Man can become more directive of his affairs and can, to a larger degree, control his destiny.

I would like to dwell further on the computer development as an extension of the "industrial revolution." This implies the growing complexity of our technology and our social organization. This in turn increases the total task confronting the educational agencies of society. More people must receive more education.

About fifty years ago one engineer was employed to 250 factory employees. Today this ratio is one engineer to less than 50 employees. This means that a greater number of people must be trained in the basic skills and concepts of our technological culture.

In order to meet these severe educational tasks, it will be necessary to revise courses of study, introduce new subjects, and improve our skill and efficiency of teaching. It will be necessary to devote more attention to the education of the basic sciences in the high school and even in the grade school. We must demand that grade-school teachers, for instance, know something about arithmetic and how to teach it.

We have heard a great deal about the place of mathematics in this new technology. I am sure that not all of us expect a great number of people to obtain Ph.D.'s in mathematics. However, there can be no question that the application of the computer will require a greater degree of quantitative and logical thinking. The computer is a mathematical and logical machine whether it is applied to the solution of engineering problems or to the processing of data in a complex business system. Furthermore, additional areas of application must be formulated in terms of quantitative models. Hence, in this broad sense, mathematics is necessary and fundamental. Consequently, more people must receive better education in this fundamental science which will train people to think clearly, logically and quantitatively. In this broad sense, then, mathematics is coming to the forefront as a central discipline of our time. For it provides the structure on which information can be displayed and it provides the symbolism and mechanism to express dynamic relationships in a large system.

We are thus witnessing the emergence of mathematics as one of the basic industrial sciences with great social utility and import. Therefore, mathematics education is of great concern to all of us. At this point I wish to mention one of the trends among the professional mathematicians which I believe is harmful to the improvement of mathematical competence in our people. Here I have in mind the tendency among mathematicians to withdraw into abstractions and purely axiomatic methods. I believe that mathematics should be taught, especially in the early stages, with the aid of physical reality and in terms of sense perception. To withdraw too early into the realm of abstractions is not realistic from the standpoint of good teaching, learning, or in attracting additional students to study this basic subject.

An interesting thing is that the computer technology will increase our productivity. This in turn increases our leisure time. Hence an added task is placed on our educational system to educate people to make proper use of this leisure, and to live constructively and creatively during their leisure time. We have here then the need to educate a greater number of people in the skills and concepts necessary for a proper functioning of our technological society and, at the same time, to educate our people to live meaningful lives and to devote their leisure time to greater personal and social ends.

Man is being freed from the role of "the beast of burden" and to a larger extent he is becoming a coworker of the creative forces in the world.

I wish to conclude my remarks with one more comment. The greatly increased task of modern education is so enormous as to require the cooperation of all concerned. Especially it is important that programs on the local level be organized, in particular between industry and educational institutions. The Wayne University Computation Laboratory program is an example of the joint enterprise between industry and the University. Its primary objective is to provide training in the computer field in particular, and to contribute to the advancement of this new technology in general.

CHAIRMAN BONN: Thank you, Dr. Jacobson. Perhaps some of the increased leisure which will result from a widespread application of computers could be well used by having individuals help in the education of others. This would be a fruitful use of the spare time provided by increased productivity.

Is there any other panel member who would like to make a statement? Dr. Mauchly?

DR. JOHN W. MAUCHLY: I guess I'm the only one left. Well, I have listened with a great deal of interest to everything that has been said here, as you have too, I suppose. A great deal of it was provocative. A great deal of what's been said, I think, we must all agree with, but I can find some areas of disagreement already.

In the first place, just to touch on this question of education and shortages, I think that it might be a little extreme, but still be a permissible way of meeting the point, to say that our effort in improving education ought to go back to kindergarten. There was a little said about what we could do in college, and later we were talking about high school, and then the speaker just before me said that we must go back to the elementary school and the teaching of arithmetic.

It seems to me that we might go back even further than this kindergarten, to the point at which we get our first notions about what mathematics is, what numbers

are like. If we could, we would like to go into the nursery schools and into the home, and try to prepare people for this more quantitative and numerical life in their very formative stages.

Of course, when you go back that far, there isn't so much that one can do in an organized way, but it still seems to me we ought to set our sights in that direction and see what can be done. In part, this means, of course, influencing the attitudes of parents so that they themselves don't either consciously or unconsciously prejudice their children against the disciplines which we are interested in here.

As far as I have seen, a great deal of the attitude of children toward either mathematics or engineering or any of the other disciplines we were speaking of is actually influenced by the way in which the parents treat these things. So, from that point of view, anything we can do in increasing the sympathy and understanding of the populace in general toward the careers and the attainments that we are looking at would be helpful.

Now, with respect to some of the forward-looking remarks of Dr. Sayre, it is certainly true that many of us are interested in what has been given the name "artificial intelligence." This is indeed a field in which a great deal is going to be done, and there will be much influence on the future applications if we are successful in some of the endeavors which he described as coming under the "inexact" rules, procedures, and applications.

In the meantime, while some of us are carrying on research on what can be done in this inexact field, the people in the schools, of course, are hard put to it to catch up to us on what can be done in the exact field. I was rather taken with the idea suggested a minute ago that programming is an activity which is not beyond the understanding of the high-school student. A lot of us have realized this; the pregnant suggestion may be that programming and coding is good discipline, having merits comparable to those long cited by educators regarding the study of geometry.

In many cases people have said, "Well, students should study geometry, not because they are going to become surveyors or in other ways use geometry and all the theorems which they learn in the course of geometry, but because this is a good discipline for teaching them something about logic, and the way in which valid deductions can be made."

So, I'm certainly in agreement with the idea that there is a good reason for considering programming in some form as on a par with geometry in that sense. Of course, it's not too fashionable nowadays to insist on studies purely for their disciplinary value, but I think that the various committees which are now engaged in studying revision of the curriculum for high schools and elementary schools are helping to make the pendulum swing the other way and encouraging the kind of studies which have in the past been exemplified by such things as algebra and geometry.

I would like to comment on what could happen in the Patent Office if we had machines which would grind through a lot of the tedious work which now has to be done by examiners and searchers. I certainly am at variance with the opinions expressed by Dr. Forrester. It's almost as if he were to have remarked that it's too bad that the printing press was invented, in view of the voluminous literature that we have and can't read.

The purpose of the effort to introduce machine searching methods in the Patent Office is, in a sense, to decrease the number of patents issued. In other words, there are now cases in which patents have been issued which should not have been issued, just because inadequate search has not revealed the fact that some conflicts in priority have occurred. With better searching methods, we can expect that a more orderly and systematic patent procedure can be carried out.

This is not the place to argue the merits of the principles underlying the United States patent system, but if we start with the premise that the disclosures which are made under this patent system are a good thing, then it certainly is to the benefit of all that the patents can properly be searched and properly be issued. That is the aim of the efforts in introducing machine searching in the Patent Office work.

However, there are a number of other places where searching of literature is important; for instance, consider the question of what happens to all the information developed in medical work on pathology, or what happens to all the tons of printed technical material which we can't get around to reading. How do we sort through it and find out what is most pertinent for us to read?

There is a curious fact here. Many people are urging that electronic computers be used in information-searching systems when it's not at all clear that electronic computers are the most urgent need. In other words, there are many ways of doing a much better job than is now done without introducing a single vacuum tube or transistor or magnetic amplifier. Considerable improvement is possible without using even a punched-card machine.

What is really needed is plenty of effort put into the digesting and consideration of the material available, to see how the information can be keyed and classified, indexed, or any other term you wish to apply here, so that it can be later retrieved, and this initial work as to keying the information is something that really requires an intelligent being who understands the subject matter.

It may be that ultimately the "artificial intelligence" which we have been discussing will be able to reduce some of that load, but it will be quite a while before that's done. In the meantime, there are some other developments which haven't been mentioned today, which I certainly would like to see, such as devices which can recognize printed characters and automatically translate the printed word into magnetic-tape records or other machine media, so that much of what has been

printed can be fed into computers with a minimum of human effort.

We won't be able to ask the computers to evaluate such records in the same sense that the human being evaluates them for a good while yet, but a large body of information already in print will be useful to us because we have already evaluated it. It is the hard and costly work of getting it into the computer that is stopping us.

I might make one more comment, and that is that I'm certainly in agreement with the thought that a computer in a university setting should play somewhat the role of the general university library. I was struck by some remarks that Dr. Aiken made to me at Harvard not so long ago as to the way in which his contacts with all the rest of the university were aided by the fact that he was in the computing laboratory, that he actually had, I think he said, as much contact now with the professor of this or that language—or a professor of ancient history—as he had with the physicist next door.

Incidentally, not all of these electronic computing devices have been sponsored by or instigated by the requirements of physicists. In fact, it's been necessary several times in the past to remark that the physicists and the engineers have been as slow as anyone to make use of these facilities. Computers have been used, as they should be, in a diversity of other activities and if anything, the engineers and the physicists are somewhat lagging in their use of them.

Then, finally, I will close with a comment on an interesting bit of phraseology which Dr. Astin used. He spoke of the various organizations coming to the National Bureau of Standards and asking what areas of work they might have which were applicable to electronic computers. I don't know whether that phrase was accidental or very deliberate, but so often we have the question asked: are these electronic computers applicable to this area of work? It seems quite reasonable to me to ask the question the other way around, in the phrase that Dr. Astin used: what areas are applicable to these computers? That is, what areas can be so treated that they can be handled by computers?

The willingness of an organization to change its way of life, so to speak, so as to accomplish on the computer an ultimate end result formerly accomplished some other way, is quite a factor in promoting the application of these machines. If they are stiff and unbending and say, "We must do everything exactly as we did before," then the computer may be an inefficient solution to their work; but if they are willing to see that a modification of methods will get the same end product, they may find the computer is much more efficient for the purpose.

That's all I have to say right now.

CHAIRMAN BONN: Much as I would like to give the various members of the panel an opportunity to answer and review the arguments which have been raised, I think that you who have sat so patiently through these talks now deserve a chance at the floor. I would like anybody who has a question to raise his hand, and I will try to recognize you. Please state your name, company affiliation, and to whom your remark is addressed. I see Dr. Grosch's hand is raised.

DR. HERB GROSCH (*General Electric Company*): I guess I'm going to talk mostly to Forrester and Cohen.

I'd like to point out to these two gentlemen and to others that they are probably overlooking the extreme potential of the industrial users of this equipment in this field. Universities led the pack in the late '30's and early '40's, and government led the pack in the middle '40's, but since then the destinies of the computer field have been directed by the industrial and business users, with the government tagging along and the universities lagging far, far behind.

I would like to second, for instance, Dr. Cohen's fine idea that in a university a computation laboratory is parallel to a general library, but I would point out that with the partial exception of Harvard—and even at Harvard the course of work is given in the Department of Applied Science, rather than in a separate organization like a school of library science—no university has actually done this yet, whereas in my part of General Electric the computer activity is parallel to engineering, manufacturing, and accounting, and serves all those areas, and it is perhaps no accident that the group involved also operates the library system.

And in another part of General Electric the largest and most imaginative attempt to integrate engineering, manufacturing, and accounting as a single giant computer program is already well under way, far in advance of any similar activity in any university or government institution.

Now, I think it's an important thing, for instance, that we are going to stick entirely with the Cohens and the Forresters and John von Neumanns and not have any of us working stiffs represented in these groups that are working ahead. End of question.

CHAIRMAN BONN: Before I give Dr. Forrester and Dr. Cohen a crack at this, I'd like to say that as a producer of electronic computers we also train people. We hire mathematicians and train them in programming. We hire electrical engineers and train them in the design and maintenance of machines. Then along comes a customer to hire them away from us and do his job.

DR. GROSCH: Not me! We train them ourselves and send them to your schools as a reward afterwards, as a social present.

CHAIRMAN BONN: Would you like to answer this?

DR. FORRESTER: I'm not sure that I detected a question. I thought Dr. Grosch made a statement, and I don't differ with the statement. Have you really got a question, Herb?

DR. GROSCH: No, I don't really think so, Jay. It was just a polemic.

DR. FORRESTER: On this relationship of the field to business applications that I have spoken of and that Dr. Grosch just mentioned, I think there is a parallel or an analogy that is worth giving some thought to. If you

go back about 20 years, engineering and the sciences were relatively separate from one another. It has been since 1938 that the great laboratories and the new electronic developments have grown at a very rapid rate. This renaissance in engineering resulted from a merging, once again, of mathematics and science with engineering. In the preceding several decades, engineering had drifted away from its scientific foundations and had become something of a cookbook art. We are due for a similar major change in industrial management as science and engineering techniques begin to merge with the social sciences and economics.

CHAIRMAN BONN: Dr. Cohen, would you care to make a comment?

DR. COHEN: Well, I would like simply to use the old phrase of Mae West and ask Dr. Grosch to "come up and see us sometime."

CHAIRMAN BONN: Any other questions?

MR. WALTER (*Naval Air Matériel Center*): I think I'd like to address my remark to Dr. Forrester.

I think in some respects we have a short-sighted view by just saying we want to teach computers or computer techniques or programming in the high schools and elementary schools, and so forth. I think our salvation has been found in that we were able to take an economist or a mathematician or a good physicist, one that was skilled in the basic sciences, and we were able to make him a good computer man. So, our salvation is to stress the basic sciences, and not worry about computers or digital techniques, but teach them physics, mathematics, and teach them English, how to express themselves, and then transfer that knowledge.

For example, many people get out of college in engineering, and they go into an entirely different field. They may be trained as mechanical engineers, and go into aeronautical engineering, and if you are trained in the basic sciences you can easily transfer to the different fields.

DR. FORRESTER: I agree with you completely, and I don't think it's at all in conflict with what I meant.

The point is that one would introduce some of the techniques as sidelights, as completely incidental things here and there where the opportunity arises. In the undergraduate courses one uses the slide rule. Why not recognize the existence of a digital computer when the occasion is timely, as when the instructor covers step-by-step integration in calculus?

I do not mean that there would have to be a separate computer course in high school, maybe not even in the undergraduate curriculum. We should just recognize the importance of information flow and its processing as an important factor in everyday living. I agree with you, except that information handling in its broadest sense is one of the basic sciences.

MR. LIPPEL (*Signal Corps*): I have two questions. The first is for Dr. Sayre. Dr. Sayre mentioned about having the machines perform intelligent operations—I don't remember the phrasing—and also talked about the amplification of problems given to the machines, of solving them in an extended sense.

I don't know exactly what he means by that thing. Does he mean that the machine will use imagination and inventiveness and do something and solve a problem that is not the sum total of the problem given to it by the programmer, and put into the machine by the designer?

DR. SAYRE: I think I'd answer your question as follows. I would envisage placing a machine in an environment which it can affect by its actions and from which the consequences of its actions are fed back to it. It would begin with a procedure that had been given to it, but it would at the same time execute neighboring procedures and test out by its interaction with its environment whether one of the neighboring procedures might not be more successful than the one it had executed; after enough favorable evidence it would adopt this procedure.

This might be one approach to endowing a machine with something that approaches intelligence.

MR. HOWARD CARRUTHERS (*IBM*): I'd like to ask Dr. Astin if he would remark, as it's not clear in my mind—he explained some of the efforts in the National Bureau with regard to machine building without indicating as to why machine design is not possible on commercially available machines or cannot be simulated by these machines, and also whether this is a short run, or to put into it more free thinking or free operation, not biased by the specific machine.

DR. ASTIN: I think you are referring to my discussion of the data-processing machine which we are now designing and planning to have built to aid us in the advisory services that we give to other government agencies on adapting their operations to the machine techniques.

Our primary objective in this is, of course, to promote greater efficiency and effectiveness of government operations in the office-management field, with such things as inventory control, record keeping, or even information storage and retrieval. Here what we want is a pilot machine which we can use in making operational studies on the problems of another agency, and attempt to arrive at an optimum machine system for this agency.

In order to accomplish this, our machine must have as one of its major attributes extreme flexibility. A particular example is in simulating the input equipment of a variety of commercially available machines, all of which have incompatible methods of representing and storing data. Our machine must have sufficient flexibility to represent any of the commercially available machines, and what we expect to do then is come up with recommendations for a particular existing machine as being optimum, or an existing machine with modifications, or a combination program of computing machines from different manufacturers, or a combination of components, or even a specification for a completely new machine.

CHAIRMAN BONN: We have time, unfortunately, for only one more question. Is there another question?

MR. R. S. OULD (Washington, D. C.): As to machine searching in the Patent Office, I would like to point out what the people not connected with the Patent Office may not realize, and that's the question of the type of personnel that are going to do the encoding. If that thing gets started, it's pretty likely to break down, from having clerical people do the encoding instead of trained examiners, and with that in view it's pretty sure that it will not work.

Even with the few arts in which it is recognized—for instance, certain fields of medicine—that are best adapted for this type of searching, the question is: who is going to do the encoding and keep it up to date?

CHAIRMAN BONN: Well, I'm sure that we will have to trust the judgment and skill of the people who are working in detail to perform the encoding and do the job in a reasonable manner.

I see that we have passed our time limit already, and I would like to suggest that we all give a rising vote of thanks to our speakers and panel members. Thank you.

Some Automatic Digital Computers in Western Europe*

NELSON M. BLACHMAN†

INTRODUCTION

WHILE IN EUROPE to attend the Information Theory Symposium[1] in London and the Analogy Computation Meeting[2] in Brussels in September, 1955, I visited a number of European digital-computer laboratories, including those of the British Radar Research Establishment, the Swedish Board for Computing Machinery, the Danish Institute of Computing Machinery, the Norwegian Computing Center, the Institute of Technology in Munich, the Swiss Federal Institute of Technology, IBM France, the Compagnie des Machines Bull in Paris, and the Bell Telephone Manufacturing Company in Antwerp. The choice of these particular laboratories was based on the significance of their work, convenience of fitting them into my itinerary, and on my having seen only one of them on my trip to attend the 1952 Information Theory Symposium in London. Fortunately, I was in Brussels and in Paris just at the times of national exhibitions of office equipment. I was therefore afforded an excellent over-all view of the state of the art of digital computation in Western Europe, although this trip included only about a third of the Western European laboratories carrying on significant work in the digital-computer field.

The computer laboratories of the Radar Research Establishment, Great Malvern, England, are only two of the dozen or so British organizations carrying on advanced work in this field. Except for the Soviet Union, about which little is known, Britain is second only to the United States in the magnitude and quality of its computer work. Sweden or Germany might rate third, followed by France, Japan, the Netherlands. Canada, Australia, Switzerland, Belgium, Italy, Norway, and Denmark.[3] At a computer meeting held in Darmstadt, Germany, in October, 1955, computers were revealed in Czechoslovakia, the U.S.S.R., and perhaps Poland.[4] In the field of punched-card machines, Europe is not far behind the U. S. The two business machine exhibitions showed France and England to be doing very well in this field, and Belgium to be well supplied with such machines, mainly from outside Belgium.

RADAR RESEARCH ESTABLISHMENT

The Radar Research Establishment (RRE) is located in Great Malvern, Worcestershire, about ninety miles west-northwest of London, in the beautiful Malvern Hills, and almost on the Welsh border. About two years ago it was formed by the consolidation of the Telecommunications Research Establishment (TRE) and the Radar Research and Development Establishment (RRDE). Because each of these establishments had its own digital-computer laboratory, RRE has two,

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[1] N. M. Blachman, "The third London symposium on information theory," IRE TRANS., vol. IT-2, pp. 17–23; March, 1956.

[2] N. M. Blachman, "The international meeting on analogy computation," IRE TRANS., vol. EC-5, pp. 36–41; March, 1956.

[3] N. M. Blachman, ed., "1953 ONR Survey of Automatic Digital Computers," PB 111 293 Office of Tech. Serv., Washington, D. C.; 1954.

[4] A. S. Householder, "Digital computers in eastern Europe," *Computers and Automation*, vol. 4, p. 8; December, 1955.

separated by a distance of some three miles. In one of them is the TRE COMPUTER, which was built on the premises by TRE; in the other is the MOSAIC (Ministry of Supply Arithmetical Integrator and Calculator), whose logic was designed by the National Physical Laboratory, Teddington, whose circuitry was developed by the Post Office Research Station, London, and which was constructed by the All-Power Transformer Co. It has been in operation since December, 1952. RRDE was a Ministry of Supply laboratory, like TRE and RRE; hence its computer actually belongs to the Ministry of Supply.

The MOSAIC occupies twelve tall relay racks, arranged in a horseshoe, with spaces between them to walk through. Chassis are mounted vertically in the racks, cooled by air blown from a duct. The mercury-delay-line internal store, containing 64 sixteen-word tanks and several shorter tanks, is in another room, and a third room contains the control position—a desk with an electric typewriter and a small box with control keys on top. In addition to the typewriter, Hollerith punched cards are used for input and output. The use of the computer is allegedly made simple and convenient by a "code book," which describes the MOSAIC's library of subroutines.

Originally, the MOSAIC was required for the solution of one particular problem in the analysis of radar data, but it turned out that a completely flexible general-purpose computer would best serve this application. The MOSAIC is a serial, binary machine, using $3\frac{1}{2}$-address instructions. The internal memory has a capacity of 1040 forty-binary-digit words. Its clock frequency is 570 kc. It can add two numbers in 70 microseconds (exclusive of access time, spent procuring the numbers) and can multiply in 6 milliseconds; division is not built in but must be programmed. The MOSAIC uses about 6000 tubes and 2000 germanium diodes, and it consumes 30 kw of power.

The TRE COMPUTER, in operation since early 1954, is smaller and more compact, using 2000 tubes and 1000 crystals, and consuming 10 kw. It operates in the parallel mode, and its internal store is of the Williams focus-defocus type, using 24 cathode-ray tubes, one for each binary digit in the word. The clock frequency is 50 kc, obtained from a phonic wheel on the drum. The computer occupies six racks, the circuitry for two digits occupying either side of each rack. The control console is in a separate room, where the teleprinter tape reader and punch for input and output are also located. Instructions, which are of the one-address type, include a number of different logical operations but neither multiplication nor division, because the original intention had been merely to gain experience with computer circuitry. A subroutine of 27 instructions is generally used for multiplication, which causes an average of 357 operations to be performed over a period of 14 msecs, but a faster multiplication program, containing 41 or 47 instructions, is available; the latter causes an average of only 275 operations to be executed, taking 11 msecs.

R. H. A. Carter, who is in charge of the computer, has in mind to incorporate a multiplier capable of 120-μsec multiplication, since, in spite of the computer's original purpose for engineering experimentation, RRE's mathematicians have pre-empted the machine for computation. On the basis of his experience with Williams storage, Carter, like many others, would prefer a magnetic-core store: the cathode-ray tubes have been too short-lived. Earlier plans to expand the TRE COMPUTER's internal store from 512 to 1024 words have been abandoned because of difficulties with read-around ratio, which is no problem with 512 words, being over 256.

The TRE COMPUTER is unique in its use of two wires to transfer each binary digit, one for "0" and the other for "1." Similarly, each register uses two flip-flops per digit, of which only one must be flipped. Thus, circuit failures nearly always produce *no* result rather than an error. Another unique feature of this computer is its parallel magnetic-drum external store, which so far had not been connected to the machine. The drum is 4 inches in diameter and 9 inches long. The 28 read-write heads (4 for picking up timing marks) on this drum are mounted on a bridge which is able to move parallel to the axis of the drum.

The bridge formerly rested against a cam which was driven by a worm gear, so that each head would cover a 32-turn helix and then, during the following 32 revolutions of the drum, would be returned to the starting position without reading or writing. Thus, since the drum speed is 1500 rpm, the average access time would have been 1.28 seconds. To reduce the average access time, circular tracks are now used, the bridge being positioned over any of the 32 sets of tracks by five relays, one of which moves the bridge 160 mils, one 80 mils, etc., down to 10 mils, the spacing between adjacent tracks. In the positioning of the bridge, an accuracy of 2 mils is expected to be sufficient, but a 1-mil repeatability is anticipated. Transfers between the drum and the main store will be in blocks of 64 or 128 words.

In the TRE COMPUTER, except on the cathode-ray tubes, no plugs or sockets are used; all connections are soldered. As a result, no difficulties have been experienced with poor connections except on the cathode-ray tubes.

According to P. Taylor, the TRE COMPUTER's chief programmer, the digit-by-digit operations "logical sum" (sometimes called "inclusive 'or' ") and "sum modulo 2" ("exclusive 'or' ") are seldom used, but much use is made of the "logical product" ("and"). The TRE COMPUTER is reputed to be easier to learn to program than the MOSAIC, and most users do their own programming, often contributing new routines to the computer's library in the process. Thus, three programmers work for the MOSAIC and only one for the TRE COMPUTER. These two machines are usually run ten or

twelve hours a day, starting at 8:00 A.M. At the end of this time the MOSAIC is shut down for the night, since it can't be trusted unattended, but the TRE COMPUTER is run until it breaks down.

The Swedish Board for Computing Machinery

The Working Group of the Swedish Board for Computing Machinery (Matematikmaskinnämndens Arbetsgrupp) in Stockholm has constructed two computers. The first, the BARK (Binär Automatisk Reläa-Kalkylator), a relay computer with plugboard programming, was completed at the beginning of 1950 and has recently been dismantled. The second, the BESK (Binär Electronisk Sekvens-Kalkylator), a general-purpose computer, completed in March, 1954, proved to be a thousand times as fast and in much greater demand. In many respects the BESK is similar to the TRE computer, but in detail it resembles more closely the Institute for Advanced Study (Princeton) family of computers, whose logic it copies. However, the circuitry is the BESK's own. The BESK is of very neat construction and is housed in a good-sized room on the second story of the old building of the Royal Institute of Technology (Kunglig Tekniska Högskola) on one of the larger streets of Stockholm. The BARK formerly occupied a room on the first floor of the same building, but nothing remained of it but its framework at the time of my visit in October.

The BESK's word length is 40 binary digits, it operates asynchronously in the parallel mode using one-address instructions, and its internal memory is of the Williams electrostatic type, storing 512 words with an access time between 12.5 and 25 μsec. Two magnetic drums 4.75 inches in diameter by 13 inches long, turning 3000 rpm, provide a serial external memory of 8192 words, with a block of 32 words on each of the 256 tracks. Addition takes 1 or 2 μsec plus access times; multiplication takes 250 μsec, and division, taking 600 μsec, has recently been incorporated. The BESK uses 2250 tubes and 200 crystal rectifiers; its power consumption is 14 kw provided by a six-phase supply regulated by thyratrons to 0.5 per cent. Stockholm's climate permits the use of fresh air for cooling all year long.

A punched-tape reader making use of the dielectric properties of the tape is used for input; it reads 400 five-bit characters per second, four positions being used for information and one to signal "read" or "don't read." A single-tube 100-kc oscillator feeds its output to all five positions across the tape. For each position, a one-tube amplifier and detector in a bridge circuit develop a 30-v output if there is no hole, the circuit being balanced for zero output where the hole is punched.

An electric typewriter is used for output at 10 characters per second. In addition, the laboratory of the Swedish Board for Computing Machinery has recently developed and connected to the BESK a tape punch that punches 170 characters per second, and Erik Stemme, chief engineer of the laboratory, feels that this speed can be doubled! For output the BESK also has on its control console a seven-inch cathode-ray tube graph plotter which accepts 9-binary-digit numbers (0.2 per cent precision). Work is also under way on magnetic-tape storage, using the Potter tape handler and Brush magnetic heads.

The BESK's electrostatic store makes use of the circle/dot representation. The 512-spot raster is arranged in the form of a thick + superposed upon a square. In addition, there are eight spots below this raster which are used for beam-current regulation, It is felt that this crt store is unduly sensitive on account of its low signal-to-noise ratio, though it is considered to be otherwise satisfactory. This store is to be replaced by a 1024-word magnetic-core matrix memory.

The BESK is run 24 hours a day, five and a half days a week, with 4 hours a day scheduled for maintenance. Of these 4 hours, 3 are devoted to the Williams memory. About 85 hours a week of good computing are obtained. No difficulty whatever is found with the circuits; all breakdowns have been traced to tubes. Thus, the spare arithmetic-unit chassis, for example, has never seen any use.

The BESK is available for use by Swedish industry, which accounts for over half of its work load, as well as by science and the government. The charge to industry is 240 crowns (about $45) per hour. The Swedish government also pays for its use of the BESK, but scientific problems, which constitute about 10 or 15 per cent of the BESK's work load, are put on free with the approval of the Board. Weather forecasting computations for the government take up 3 or 4 hours every day on the BESK and represent one of the important scientific applications of this machine. The partial differential equations describing the movement of the atmosphere are dealt with as difference equations on a grid of 32 by 40 points which represents an area extending from North America to Europe and from North Africa to Greenland.

The BESK's clients do their own programming; the BESK's mathematical staff of six devote their efforts mainly to work on library programs for the machine. The engineering staff consists of seven or eight people, but the construction of the BESK was originally undertaken by a group of only four engineers in 1947, namely, Fröberg, Kjellberg, Neovius, and Stemme, some of whom spent some time with the Harvard University and the Institute for Advanced Study computer projects.

The laboratory of the Swedish Board for Computing Machinery must be ranked among the four or so most outstanding organizations in the digital-computer field in Europe. Unfortunately, although the Mathematical Working Group has been hoping to see itself and its laboratory established on a permanent basis, as of the time of my visit, it was still operating from year to year.

The BESK is heavily overloaded with work, having been in demand 38 hours more than were available during the week of my visit. The SAAB aircraft com-

pany, which accounts for a large part of the BESK's industrial work is to build a copy of the BESK in Linköping for its own use. This computer, to be known as SARA (SA for SAAB and RA for Rekenautomat, "automatic computer"), is expected to take something over a year to complete.

Another copy of the BESK, to be called SMIL (Siffer-Maskinen I Lund, the digital machine in Lund), will be built at the University in Lund, Sweden. Its construction, too, is expected to take over a year. SMIL's drum will operate in the parallel mode, there being 2048 words stored on an 80-channel drum, with provision made for attaching another similar drum. This drum, turning 6000 rpm, will serve as SMIL's internal memory, there being no electrostatic store. The average time required to execute a one-address instruction will be 7.5 msec. Only SMIL's arithmetic unit will be identical with the BESK's.

It is interesting to note that the names of all four Swedish digital computers are four letters long and have meaning as words; BARK means the covering of a tree trunk, BESK means "bitter," SARA is a girl's name, and SMIL means "smile."

Danish Institute of Computing Machinery

Still another copy of the BESK is to be built in Copenhagen at the Computing Center (Regnecentralen) of the Institute of Computing Machinery (Matematikmaskininstitut) of the Danish Academy for Technical Sciences (Akademiet for de Tekniske Videnskaber). Bent Scharøe Petersen is in charge of the construction of the computer, and Dr. Thøger Busk will head the mathematical group. The project has the guidance of the Danish Working Group on Mathematical Machines, whose chairman is Prof. Richard Petersen of the Applied Mathematics Laboratory at the Danish Instiute of Technology (Danmarks Tekniske Højskola, DTH). The other members of the Working Group are Profs. Rybner and J. Oskar Nielsen of the Institute of Telecommunication.

Having the complete plans of the BESK at their disposal, the Working Group feels that their resources, equivalent to $125,000, will suffice to complete the machine by the fall of 1957, though at the time of my visit Scharøe Petersen himself constituted the entire engineering staff, and the first meeting of the Working Group was yet to occur. The addition of three electrical engineers and two technicians to the staff was being considered. Two more mathematicians will be added to the staff later, but users of the computer will be expected to do their own programming and coding. To make this possible, the DTH is setting up courses on the use of automatic computers.

The computer is to incorporate the ferrite-core store being developed for the BESK. The Danish computer's accumulator will be extendable to 80 bits for full-length multiplication by combining the accumulator and the multiplier register. Unlike Sweden, Denmark has no aircraft industry to keep its computer busy, but its use is anticipated on problems associated with nuclear reactors. Initially, the construction of the computer is being undertaken on the top floor of the Telephone Company building in Copenhagen, about three miles west of the DTH, but is to be moved later to permanent quarters.

The Danish Academy for Technical Sciences is a private organization founded in 1937, supported by the Danish government, industry, etc.[5] Important among these sources are the profits made by Carlsberg beer. The academy distributes its funds among its various research institutes, whose fields include acoustics, geology, microwaves, optics, radio, refrigeration, textiles, timber, welding, etc. Their work includes fundamental studies as well as applied investigations for Danish industry. The Academy's headquarters, which are located in one of the bildings of the DTH, are looked after by its Secretary, Bjerre Lavesen.

Since 1951 the DTH Applied Mathematics Laboratory has had in operation an eight-integrator mechanical differential analyzer, which was built by the combined efforts of Danish industry and the DTH at a cost of about $25,000. It is equipped with two curve followers/plotters.

I was shown some very interesting work at the Copenhagen Telephone Company, where the electronic computer is to be built, involving the generation of random binary digits for use in telephone traffic-handling studies. A scintillation detector of radioactivity is gated into a counter for a fixed period of time, so that a large number of pulses is counted. The parity of this count (even or odd) then provides a random binary digit. To avoid the possibility of bias in the counter, however, the process is repeated immediately, and only the combinations even-odd and odd-even are used, giving a random binary digit 0 or 1, respectively. The combinations even-even and odd-odd are ignored. The same counter is used in both instances, and it is reset to zero each time, so that if its characteristics do not change over the interval between the two counts, 0 and 1 are exactly equally likely. In this way, from 1000 to 5000 random digits are obtained per second.

Norwegian Computing Center

With the support of the Board for Mathematical Machines of the Royal Norwegian Council for Scientific and Industrial Research, the Central Institute for Industrial Research (Sentralinstitutt for Industriell Forskning), located at Oslo University in Blindern, just outside Oslo, has established the Norwegian Computing Center (Norsk Regnesentral). Dr. Ernst S. Selmer of the University's Institute of Mathematics and Mechanics showed me the Computing Center, of which he is in

[5] "The Organisation of Applied Research in Europe, the United States, and Canada, Vol. II: Applied Research in Europe," the Organisation for European Economic Cooperation, Paris, France, 1954.

charge. In the latter part of 1953, at a total cost of 250,000 crowns (about $35,000), this organization completed a small binary serial magnetic-drum general-purpose computer which has been named NUSSE, a Norwegian girl's nickname. The "N" means "Norwegian," the "U" means "universal," and the remaining letters add up somehow to "digital computer," though Dr. Selmer did not know their precise significance. NUSSE is patterned after the APE(X)C at Birkbeck College, London, built by Dr. A. D. Booth, from whom the drum and some of the registers were obtained.

NUSSE's drum stores 512 32-binary-digit words, with a mean access time of 8 msec. The computer uses about 420 tubes and 200 crystal rectifiers, consumes 2 kw, and occupies a floor area two-by-three meters. Its instructions are of the two-address type, and its clock rate is 40 kc. The usual orders are built into the computer with the exception of division. A 50-line-per-second paper-tape reader is used for input, and a tape punch and teleprinter are used for output. NUSSE's staff consists of one engineer and two coders.

NUSSE has been found inadequate to fill Norway's need for automatic computation; the Norwegian Defense Research Institute (Forsvarets Forskningsinstitutt) in Kjeller, some fifteen miles from Oslo, is therefore procuring from England a Ferranti Mark II computer with built-in floating-point arithmetic and serio-parallel cathode-ray storage. At the Norwegian Institute of Technology (Norges Tekniske Høgskole) in Trondheim, a digital differential analyzer named DIANA has been built at a cost of 30,000 crowns ($4300).

Although not a great deal of research has been done in Norway in the digital-computer field, Norway is in close touch with developments in the United States. Dr. Selmer has worked on the CALDIC at the University of California, Berkeley, and on the Institute for Advanced Study Computer, and in 1952 he designed the logic of the Datatron for the Consolidated Engineering Corporation in Pasadena.

Scientific research in Norway is financed in a unique manner by a regulated football-pool monopoly. Of its annual profits, about $1.5 million are used to support athletics, and the remaining $7 million provide the major part of the funds for scientific research.

Institute of Technology in Munich

The construction of the PERM (Programmgesteuerte Elektronenrechenmaschine, München) was completed in the summer of 1955 by the Münchener Arbeitsgemeinschaft für Elektrische Rechenanlagen in the Institut für Elektrische Nachrichtentechnik und Messtechnik of the Technische Hochschule in Munich. At the time of my visit the PERM was therefore being debugged. The computer was shown to me by H. O. Leilich of the Institut für Elektrische Nachrichtentechnik und Messtechnik. The computer itself, which uses 2500 tubes and 2000 crystal rectifiers and consumes 7 kw, consists of about a dozen narrow racks lined up together, with small cartoons filling unused holes in the front panel. These cartoons depict electrons thinking and computing; they belie the thesis that Germans are humorless. Along another side of the roughly twenty-by-forty-foot room stand another four breadboarded input-output racks coupling three teletypewriters to the computer.

The PERM is a binary, parallel, magnetic-drum computer using a fixed or floating binary point and one-address instructions, each instruction taking up a full 50-digit word. Its drum is the fastest currently in use, turning 250 rps, to yield a maximum access time of 4 msec. It stores 8192 words in the parallel mode on 200 tracks, with a storage density of 165 digits per inch, using "return-to-zero" recording. The drum, which is 8 inches long and four inches in diameter, operates quietly enough that normal conversation is possible right next to it. The head-to-drum spacing is 0.02 millimeter (0.8 mil) and is held to 10 per cent. To accomplish this, it is necessary to enclose the drum in a housing that ensures a uniform temperature. The bearings are spring loaded to avoid variations due to wear. The clock frequency is 500 kc, but it can be halved, if necessary, to obtain more reliable operation at half the arithmetic speed.

Fixed-point addition required 4 to 8 μsec exclusive of access time; multiplication and division take 100 to 1000 μsec. Binary-decimal conversion and an input routine are also built into the PERM. In its floating-point representation of numbers, 9 digits are used for the exponent and 41 for the factor. Instructions consist of 4 sets of 4 binary digits, each of which has a particular significance, for the order code; 13 digits for the address; 2 digits to indicate the type of address interpretation; and 19 unused digits, of which 8 must be ones. There is a "B" register which can be used, according to the address-interpretation digits, to modify the address during read-in or during execution. In a third address-interpretation mode, the computer looks at the address specified in the instruction to find the address to use in executing the instruction.

Three types of floating-point multiplication are being studied and may be built into the PERM: 1) normalization of the factors only *before* the multiplication; 2) the usual type, with normalization after multiplication; and 3) representing a number having n significant figures by a string of zeros followed by the n figures, and giving the product the same number of significant figures as the less accurate factor so that the result of a long series of calculations is obtained with an indication of its accuracy.

The mathematical group associated with the computer is also investigating various approaches to the utilization of a library of program tapes. According to Drs. F. L. Bauer and K. Samelson of Mathematisches Institut of the Technische Hochschule, the PERM will probably be used to do problems in gas dynamics and

networks. It may also be used for industrial problems and for defense work, but no such work had yet been arranged, and the group hoped to be able to confine themselves to academic research.

I was informed that the Max-Planck Institutes in Göttingen are soon to be moved to Munich, bringing their computers G1, G2, and G3 with them. G3 is a parallel, floating-point, magnetic-core computer. Thus, Munich should become a very important center for work in the computer field.

Swiss Federal Institute of Technology

The Swiss Federal Institute of Technology (Eidgenössische Technische Hochschule, ETH) is the only organization of university standing maintained by Switzerland as a whole. Its Institute for Applied Mathematics is currently completing the construction of the ERMETH (Elektronische Rechenmaschine, ETH), whose logical design was worked out by the Institute but which was largely fabricated by Swiss industry. This computer had previously been known as "R4S," in honor of the five men who began the project in 1947: Rutishauser, Schlaeppi, Speiser, Stiefel, and Stock. From 1950 until April, 1955, the Institute had the Z4, a slow binary parallel relay computer with a 0.5-second access-time, 64-word mechanical store and a punched-tape program control, which was built by Zuse. This computer is now in use by the French government, which finds it extremely reliable and useful even though the arithmetic operations take up to 5 seconds.

The ERMETH is a serio-parallel, decimal, floating- and fixed-point computer with magnetic-drum storage. It uses 1200 tubes and 500 crystal rectifiers and consumes 20 kilowatts. There are fans for cooling in the eight or ten, 8-foot-high double-doored cabinet, and the 25-foot-square room in which these cabinets are lined up across one corner is air-conditioned. All of the components are contained in 2-tube plug-in packages; there is nothing but wiring behind the vertical panels into which these packages plug. In addition, the room contains a control desk, power supplies, and input-output equipment. Punched cards are used at a speed of 8 words per second, and there are two printers, one operating at half a word per second, the other at two words per second.

The word length is 14 decimal digits plus sign, 2 seven-digit one-address instructions being fitted into one word. In the floating-point representation, three digits are used for the exponent, which can range from -199 to $+199$, the remaining digits representing the factor. Decimal digits are represented by the 2*, 4, 2, 1 code. Coding for the ERMETH is facilitated by a coding desk like the one used with the Harvard Mark IV.

The drum stores 10,000 words on 200 tracks in the serio-parallel mode, the 10-inch-in-diameter 15-inch-long drum turning 6000 rpm. A 10:1 interlace is used on the drum, so that the 300 kc drum frequency is reflected in a 30-kc clock rate. Floating-point addition requires 5 milliseconds exclusive of access; multiplication takes 20 ms, and division 40 ms. All transfer operations are automatically checked. As of the time of my visit, it was anticipated that the computer would be in operation by April, 1956.

According to Heinz Rutishauser, the ERMETH, when it is in operation, will be put to work on: refined relaxation methods for the solution of second- and fourth-order elliptic differential equations relating to problems of elasticity; ordinary differential equations relating to the stability of servos, such as would be found in a beam-riding guided missile; also eigenvalue problems, such as arise in the determination of the critical angular velocities of rotating shafts, quantum-mechanical eigenvalues relating to molecular structure, and the natural frequencies of twisted rods. These problems come from the ETH, from Swiss industry, and from the government.

Rutishauser himself has studied the stability of integration methods for ordinary differential equations and techniques for automatic programming. Some of his ideas along the latter line are similar to IBM's FORTRAN for the translation of formulas. Rutishauser would like to set up a universal language in which mathematicians and programmers can communicate. At the ETH, he teaches the courses in computer programming, Prof. E. Stiefel teaches numerical analysis, and A. Speiser has taught the courses in computer electronics and switching theory. However, Speiser has recently left to head IBM's new research laboratory in Zurich, as noted below.

Laboratory of IBM France

The laboratory of IBM France in Paris conducts research in computer circuits and redesigns the IBM machines built in the U. S. to suit European needs. IBM France, in fact, supplies IBM equipment to Europe, Asia, Africa, South America, Australia, and even on occasion to Canada. Their redesigns usually are in the direction of greater variety of business forms and methods used outside North America. For example, the IBM-France 604 has a capacity of 70 program steps, as contrasted with 60 in the U. S. version; IBM-France builds a tabulator (427?) having *two* input card feeds which is not available in the U. S. They find that the combination of their 604, tabulator, and summary punch is in considerable demand and serves much the same purpose as the U. S. Card-Programmed Calculator. An American IBM 650 magnetic-drum computer has recently been delivered to the IBM service bureau of Paris for use in its computing service. Copies of this computer are to be manufactured by IBM France and it will be adapted to the addition of IBM electronic-data-processing-machine tape units for external storage.

IBM was making plans to set up a new research laboratory with a staff of thirty in Zurich in January, 1956, to be headed by A. P. Speiser, until recently at the Swiss Federal Institute of Technology. Kinberg, who

was in charge of electronics at the laboratory of IBM France, will head the work in electronics of the new laboratory, which occupies rented quarters in a brand new building just outside Zurich. Its mission will be to discover new computer components and techniques.

Compagnie des Machines Bull

The Compagnie des Machines Bull, a manufacturer of punched-card business machines, markets its machines throughout Western Europe, North Africa, and South America. Their American sales and maintenance are handled by Remington Rand, and they in turn market Remington Rand equipment in France. In fact, the Bull gang punch is used on the Sperry Rand ERA 1103 (UNIVAC Scientific) magnetic-tape-to-punched-card converter. The organization, though French, is named after Bull, the Norwegian who invented the gang printer using type wheels (as opposed to bars) and other business machine equipment.

At its headquarters, Mr. Maurice, head of the organization, and P. Dreyfus, the chief engineer and a very knowledgeable fellow, discussed their most advanced machine, the Gamma 3B, which is intended to outperform IBM's 650 Magnetic-Drum Calculator. I also had the opportunity to see the assembly line which makes the Gamma almost from scratch in a month. The letter gamma represents a *c* for "calculator," the transliteration to Greek connoting that it is electronic. In principle, there have been three gammas: a small machine, Gamma 1; a more powerful machine, Gamma 2; and the large-size Gamma 3. The development of these computers began with Gamma 2 and progressed to Gamma 3; there has never been a Gamma 1, and all Gamma 2's have now been converted into Gamma 3's.

The Gamma is evidently the first (and presently the only) magnetic-drum computer to be produced commercially in quantity on the Continent, and it is further remarkable for the 95 per cent reliability claimed. Allegedly, only 5 per cent of its operating time on a 200-hour-per-month basis is required for repairs and scheduled maintenance. As of the time of my visit, 220 Gamma 3's had been produced, 70 of them for use outside of France, in the two years they have been in production. There was a backlog of 60 or 70 orders, and the rate of production has been ten a month. Most of these machines are of the simplest type, lacking extension units for card programming; a drum; algebraic; alphanumeric, and floating-point operation; and extra electromagnetic storage. This minimal Gamma 3 costs about $30,000. The complete computer, with drum storage, was not to be available until August, 1956; it is to cost 50 million francs (about $135,000) or rent for 2 per cent per month including maintenance.

The basic Gamma 3 itself occupies a floor area 2 feet by 4.2 feet. It uses 400 tubes and 7000 germanium diodes and consumes 3 kw. The drum and other auxiliary units contain an additional 400 tubes and use another 3 kw. Punched cards very similar to IBM cards are handled by a standard reproducer for input and output at the rate of 150 cards per minute, and a standard 100-character-per-line gang tabulator may be used for output at 150 lines per minute.

The Gamma 3 is a serial, decimal machine with a variable decimal point. The internal storage consists of 4 to 7 one-word electromagnetic delay lines with five sections per digit and an access time of 170 μsec. The word length is 12 decimal digits, which may be split arbitrarily. Programs are given to the machine on a 32-to-64-step plugboard and/or punched cards and can be stored in the memory.

Instructions are of the one-address type and consist of four sexadecimal characters, the first designating the type of operation, the second the address, and the third and fourth the beginning and end of the word in the storage address in the case of split words. Three instructions are stored in a 48-binary-digit (12-decimal-digit) word, and 48 instructions are entered on a single punched card by means of efficient coding. The clock rate is 280 kc, and the Gamma 3 can add or subtract two numbers in 0.17 msec exclusive of access time; multiplication or division takes 11 to 21 msec.

Two drums are available for external storage, one 6 inches in diameter turning 5500 rpm, which stores 4096 words, and the other a foot in diameter, turning 2750 rpm, and storing 8192 words. Both are serial, have 64 tracks, and are ten inches long. Transfers to internal storage can be carried out during computation by means of a 64-word delay line, which forms an extension of the internal store. There is also a set of electromechanical counters which provide 5 to 10 words of parallel storage with an access time between 1.4 and 400 msec for use in input and output.

Dynamic flip-flops are used, pulses being 10 v with a $\pm$3-v margin. The power supply is unregulated, and it is claimed that a 25-per-cent variation in supply voltage can be tolerated. Provision for marginal checking by means of grid-bias variation is incorporated. The Gamma 3 appears to be a good competitor for the IBM 650, although more difficult to program, since it is not basically a stored-program machine, and its drum store is external rather than internal as on other magnetic-drum computers. Nevertheless, the Gamma 3 indicates that France is not far behind England in the field of automatic computers of moderate size.

Another interesting device recently developed by the Compagnie des Machines Bull is a check-sorting machine operating on magnetic-ink marks on the back of the check at a rate of 450 checks per minute. A demonstration machine operated on the basis of 12 binary digits, each indicated by the absence or presence of a $\frac{1}{8}$-by-$\frac{1}{4}$-inch black rectangle. Each check was marked with one of the 4096 possible codes and also with its complement, for checking purposes. The sorter delivers each check to one of 16 bins. It is able to handle checks that have been crumpled, but photo-electric cells

stop the machine whenever there is danger of its injuring a check.

Compagnie Générale de Télégraphie sans Fil (CSF)

While in Paris I also visited the computer laboratory of CSF, an organization perhaps more famous at present for its carcinotrons. This laboratory is located at 12 rue Carducci, Paris XIX, in the northeastern part of the city. Fortunately, the buildings on either side of this laboratory are labeled with house numbers; otherwise, I might never have found the place, which is not distinguished in any way and must be entered from the rear. This situation is not at all unusual in Paris; the American Embassy Annex to which I had to go to find Lt. Col. Chas. E. Harrison, the very helpful Signal Corps Attaché, was even harder to find, though I had been there three years previously and had its address.

This laboratory carries on research and development of prototype equipments, but the production is carried out by the associated organization Société Française Radioélectrique. Their work is entirely in the field of high-frequency (500-kc) analog-computer components, mainly for use in special applications like fire-control computers. H. J. Uffler, Technical Director of the Calculator Department of CSF, delivered a talk on this equipment at the International Analogy Computation Meeting in Brussels in September, 1955.[2]

At the laboratory, Messrs. Samuel and Précicaud showed me some of the work in progress there. A generator of arbitrary functions is being developed which provides parabolic interpolation between the points at which it is set. Also, a generator of functions of two variables has been developed which has on its roughly one-meter-square panel an array of 144 (12×12) knobs to set on as many condensers the values of the function. Another interesting piece of equipment at the laboratory is a servo-indicating capacity-measuring instrument which covers the range from 0.01 mmf to 200 mmf with an asserted accuracy of 0.01 per cent. The sensitivity of the device, which operates on 472 kc, can be increased by a factor of about 25, it is claimed, so that it will measure down to 4×10^{-16} farad.

IRSIA-FNRS Computer, Antwerp

The Belgium Institut pour l'encouragement de la Recherche Scientifique dans l'Industrie et l'Agriculture and the Fonds Nationale de la Recherche Scientifique, two semigovernmental organizations for the encouragement of Belgian applied and pure research,[5] respectively, have contributed 12 million Belgian francs ($240,000) and 10 million francs ($200,000), respectively, for the development of a large-scale serial, decimal, magnetic-drum computer somewhat resembling the Harvard Mark IV, whose plans were available. The work is being carried on at the Bell Telephone Manufacturing Company in Antwerp under the direction of W. Pouliart, head of the Electronic Laboratory, with the assistance of Dr. Marcel Linsman of the University of Liège.

The computer was completed in 1955, although its coding box, a separate piece of equipment to facilitate coding, still remained to be built at the time of my visit. It was anticipated that the computer would be moved in 1956 to a building to be constructed in Brussels which would house a Belgian statistics laboratory. Fortunately, the computer deals only with numbers, which are represented in storage by a four-binary-digit code and in the arithmetic unit by a biquinary code. If it had to speak another language, it would have to watch carefully the sharp line dividing Belgium into Flemish-speaking and French-speaking regions. Antwerp lies in the former and Brussels, thirty miles away, in the latter. At the present time, the computer's mathematical and coding staff consists of two people, but it is to be increased at the new quarters.

I was shown the computer by F. M. Michiels, who has been concerned principally with the design of the input-output equipment and the drums. The two drums, which are mounted on the same horizontal shaft, have a diameter of 12 inches and a total length of 20 inches. They have, on an aluminum base, a nickel coating on which information is stored with a density of 38 binary digits per inch on 200 tracks, half of which are used for the storage of 2000 numbers and the other half for 4000 instructions. High-impedance Permalloy-C cores are used in the heads. The head-to-drum spacing is 3 mils, and the angular velocity is 4100 rpm, yielding a maximum access time of 14 msec and a clock frequency of 98.3 kc.

Six quarter-inch-wide 500-foot circular magnetic tapes, held between glass plates, are used for external storage, input, and output, with a storage density of 250 binary digits per inch on the information channel. These tapes, which are driven at a speed of 1 meter per second by means of pneumatic clutches, have three tracks—one for timing, one for information, and the third for block marks. On both the tapes and the drums, a form of non-return-to-zero storage is used, 0 being represented by a change in magnetization and 1 by none. Three ones in a row are avoided, In addition, there is a Remington Rand typewriter for output. Two other typewriters with tape readers are to be added. Input is presently from a 10-key keyboard on the control desk that writes on tape via the computer, but it will be supplemented by the coding box.

Numbers are 17 decimal digits long plus sign; two of the digits may be used to indicate the exponent in the floating-point representation, which can range from -49 to $+50$. Instructions, which are kept separate from numbers, are of the one-address type and are 9 characters long. However, the computer is able to modify instruction addresses and is capable of both floating- and fixed-point arithmetic. Division is not built into the machine, but several interesting operations are available for handling floating-point numbers, such as replacing the factor by unity, extracting the expo-

nent, changing to a fixed-point representation, and replacing the exponent by the factor and the factor by unity. Addition takes 3 msec., multiplication between 3 and 15 msec, and division 140 msec.

In addition to the drum, the internal store contains about 20 one-word shift registers using grid-controlled cold-cathode neon tubes, which can be used at frequencies up to 80 kc but are operated in the serio-parallel mode at 25 kc, with an access time of 0.7 msec. These replace the magnetic shift registers used in the Harvard Mark IV, ostensibly because they are easier to repair. These cold tubes are also used in the operating registers of the computer. In addition, there are about 2000 hot tubes, 1000 selenium rectifiers, and 1500 germanium diodes, and the total power consumption is about 12 kw.

The computer is a dozen racks wide by 4 or more racks deep. It is assembled largely out of vertical plug-in chassis that are about 15 inches wide by anywhere from 4 to 8 inches high. On the basis of the general outline of the computer laid out by Pouliart and Linsman, five engineers developed the detailed design of the machine, and it was constructed by half a dozen technicians. Although these numbers are small by American standards, they are somewhat lavish by European standards, as is also the budget allocated for the construction of the computer.

Another group at the Bell Telephone Manufacturing Company in Antwerp, which is an International Telephone and Telegraph Company affiliate, is engaged in the development of a special-purpose digital machine for the National City Bank of New York, using computer elements similar to those in the IRSIA-FNRS Computer. The banking machine uses wider tape carrying 12 tracks. It may have fifty or a hundred 100-meter nonremovable tapes, with 4 tapes to each tape unit, all driven at a speed of 20 feet per second by the same shaft but engaged by separate pneumatic clutches. Checks are placed in celluloid envelopes, each carrying a strip of magnetic tape on which are recorded pertinent data. The machine then sorts the checks on the basis of these data, performing the appropriate computations and recording the results as each check is being handled.

Work on this machine began around the end of 1954 with a staff of two engineers. At the time of my visit, the staff had increased to 4 engineers and 4 technicians. About 7 racks of electronic circuitry had been breadboarded, and 1 tape unit and 1 control console had been built. The completion date, however, was uncertain.

Office Machine Exhibitions

Nine-day exhibitions of office machines luckily took place in Brussels and in Paris while I was in those cities. The Brussels exhibition was held in the Palais des Beaux-Arts, with 40 exhibitors, including makers of addressing machines, automatic letter openers, cash registers, coin counters, desk calculators, dictating machines, duplicating machines, filing systems, folding machines, punched-card computers, stenotypewriters, time clocks, typewriters, etc. It was quite impressive for the variety, quantity, and novelty of the exhibited equipment. Among the exhibitors, all of whom have offices in Brussels, were representatives of over two dozen brands of desk calculators. The punch-card and electronic computers represented at the exhibition included the Société Belge des Machines BULL; the Société Anonyme BURROUGHS (which was not yet marketing the E101); International Business Machines of Belgium, S.A.; Caisses Enregistreurs "NATIONAL," S.A. (National Cash Register Company, not displaying electronic computers); also Elliott-Fisher, Sunstrand, Underwood, Remington Rand, Log-Abax, and Powers-Samas (which is offering an electronic Programme-Controlled Computer; its program is held on 4 punched cards, but it has a 160-word magnetic-drum memory for the storage of numbers).

The exhibition in Paris took place in the huge exhibition hall at the edge of the city. It was quite impressive and appeared to include all that had been in Brussels and a great deal more. Whether it is by means of European skill and ingenuity or through American exportation that the exhibited machines have become available abroad, the fact remains that Western Europe has available computers which are only about a year or two behind the most advanced American machines of their types.

Correction

MORRIS RUBINOFF
Prof. of Elec. Engrg.
Moore School of Elec. Engrg.
University of Pennsylvania
Philadelphia 6, Pa.

The name and photograph of Morris Rubinoff above, were omitted from the PGEC Papers Awards listed in the June, 1956 issue of IRE TRANSACTIONS ON ELECTRONIC COMPUTERS. Professor Rubinoff was co-author with R. H. Beter, W. E. Bradley, and R. B. Brown, of the paper, "Surface Barrier Transistor Switching Circuits" (1955 IRE CONVENTION RECORD, Vol. 3, Part 4, pp. 139–144), which received the award for the most significant contribution to the electronic computer field during 1955.

Contributors

Zoltan Bay was born in Gyulavary, Hungary, on July 24, 1900. In 1923 he received the M.S. degree in physics and mathematics from the University of Sciences, Budapest, and in 1926 the Ph.D. degree in physics from the same institution. From 1923 to 1930 he was an Assistant Professor at the University of Sciences, and from 1930 to 1936 Professor of Theoretical Physics at the University of Szeged in Hungary. He also worked at the University of Berlin during 1926 to 1930. From 1936 to 1948 he was director of the Research Laboratory, United Incandescent Lamp and Electric Company of the Tungsram Company, Ujpest, Hungary, and later became technical manager of Tungsram. He also taught atomic physics from 1938 to 1948 at the Technical University, Budapest.

In 1948 he came to George Washington University, Washington, D. C., where he was a Research Professor of Physics until 1955. Since 1955 he has been employed at the National Bureau of Standards, doing research at the Radiation Physics Laboratory.

Dr. Bay is a member of the American Physical Society and Sigma Xi.

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G. W. Booth was born February 11, 1928, at Utica, N. Y. He attended Syracuse University and received the B.S. degree in electrical engineering in 1952. Following his graduation he joined the General Engineering Development Section of the Radio Corporation of America, where he participated in the development of the Bizmac system and the use of transistors in digital computer applications.

Mr. Booth is currently a graduate student at the Moore School of the University of Pennsylvania. He is a member of Eta Kappa Nu and Tau Beta Pi.

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T. Paul Bothwell (S'53–A'54) was born in Glen Ridge, N. J., on January 13, 1927. From 1944 to 1946 he served in the U. S. Navy as a radio technician. Following this, he attended the Rensselaer Polytechnic Institute, receiving the B.S. degree in physics in 1951.

From 1951 to 1954 he worked as a research assistant in medical electronics at the University of Pennsylvania, and received the M.S. degree in electrical engineering from that school in 1954. He joined the General Engineering Development Section of the Radio Corporation of America in July, 1953, and has been working on transistor applications in digital systems since that date.

Mr. Bothwell is an associate member of Sigma Xi.

Donald T. Greenwood (A'46) was born in Clarkdale, Ariz., on December 8, 1923. He received the B.S. degree in mechanical engineering from the California Institute of Technology in 1944. After duty with the U. S. Navy as a radar officer he worked for a year as an electronics design engineer for Engineering Research Associates in St. Paul, Minn. Returning to Caltech in 1947, he received the M.S. degree in physics in 1948 and the Ph.D. in electrical engineering in 1951. From 1951 to 1956 he was with Lockheed Aircraft Corporation, Burbank, Calif., in charge of their analog computing group. He is presently at the University of Michigan as Assistant Professor of Aeronautical Engineering.

Dr. Greenwood is a member of Tau Beta Pi and Sigma Xi.

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Nelson T. Grisamore (A'53) was born in Sioux City, Ia., on January 27, 1921. From 1942 to 1946 he worked for George Washington University on an NDRC contract doing research in the ballistics of rockets. In 1948 and 1950 respectively, he received the B.S. degree and the M.S. degree in physics from the University of Illinois.

Since 1950 he has been employed by George Washington University to do electronics research, and in 1954 he obtained the Ph.D. degree in physics from this same institution. Since 1955 he has been in charge of the work at the Electronics Research Project of George Washington University.

Dr. Grisamore is a member of the American Physical Society, the American Association for the Advancement of Science, and Sigma Xi.

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Rolf K. Mueller was born in Zurich, Switzerland, on August 30, 1914. He received the Diplom Physiker degree in 1939 and the Ph.D. degree in 1941 from the Technische Hochschule in Munich, Germany.

He was a research assistant at the Universities of Jena, Stuttgart, and Munich, Germany, from 1941 to 1948, and associate professor at the Technische Hochschule from 1949 to 1953. From 1953 to 1955 he was with the Air Force Cambridge Research Center. Dr. Mueller is now associated with the mechanical division of General Mills, Inc., Minneapolis, Minn.

❖

Vernon L. Newhouse (M'55) was born on January 30, 1928. He received the B.Sc. degree in physics in 1949, and the Ph.D. degree in 1952, both from the University of Leeds, England. His post-graduate work was concerned with the theoretical and experimental study of the Barkhausen effect in single ferromagnetic crystals.

In 1951 he joined the computer department of Messrs. Ferranti, where he carried out the initial development of the coincident current memory used in the Ferranti Mark II computer.

In 1954, after some months at the David Sarnoff Research Laboratories, Princeton, N. J., he joined the Bizmac Engineering Section of RCA as project engineer of the circuit design and development group. Since then he has been associated with the development of a real time computer, and is presently project engineer in charge of advanced magnetic development.

Dr. Newhouse is a graduate member of the IEE.

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Noah S. Prywes (M'55) was born on November 28, 1925. He received the B.S. degree in electrical engineering in 1949 from the Technion, Israel. He served with the Palestine Coast Guard from 1943 to 1945, and with the Israeli Navy from 1948 to 1950. After release from service he attended Carnegie Institute of Technology, where he received the M.S. degree in electrical engineering in 1951, and Harvard University, where he received his Ph.D. in applied science in 1954.

From October, 1954 to January, 1956, Dr. Prywes was with RCA, Camden, N. J., working on development of computing circuitry. He is presently with the Eckert-Mauchly Division of Remington Rand Univac in Philadelphia, where he is project engineer in charge of the arithmetic unit design of the Univac Larc computer.

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Rocco H. Urbano was born in Albany, N. Y., on October 7, 1917. He received the B. A. degree in mathematics from Union College in 1940, and the M.A. degree in mathematics from Harvard University in 1951.

Mr. Urbano served as a mathematician on problems associated with the design of fire control equipment in the aeronautics and marine engineering division, General Electric Company, Schenectady, N. Y. from 1941 to 1945. He was an instructor in mathematics at Union College from 1945 to 1948, and an instructor in mathematics at Northeastern University from 1948 to 1952. He is now serving as a part-time instructor in the graduate evening engineering division of Northeastern University, and also is chief of the applied mathematics section of the computer laboratory of the Air Force Cambridge Research Center.

PGEC News

1956 Eastern Joint Computer Conference

The 1956 Eastern Joint Computer Conference has been set for December 10, 11, and 12, 1956, at the Hotel New Yorker, New York, N. Y., reports Conference Chairman J. R. Weiner. This year's annual meeting, jointly sponsored by the IRE, American Institute of Electrical Engineers, and the Association for Computing Machinery, will have as its theme, "New Developments in Computers."

In addition to a program of technical papers, the meeting will feature exhibits by many manufacturers in the computing field. Registration fee at the conference is $5.00 for members of any of the three sponsoring societies, $8.00 for nonmembers. Advance registration is $4.00 for members, $7.00 for nonmembers. All registrants will receive a free copy of the proceedings of the conference.

J. W. Leas has been appointed chairman of the Program Committee. V. N. Vaughn is chairman of the Publications Committee. J. A. Haddad has been appointed chairman of the Local Arrangements Committee for the conference. Subcommittee chairmen are: Exhibits, A. D. Meacham; Finance, A. R. Mohr; Hotel, J. A. Grundy; Inspection, Norman Grieser; Printing, Paul Magdeburger; Publicity, A. J. Forman, and Registration, W. P. Heising.

Chapter Elections

The following chapters have reported on election of officers:

Akron—Chairman, D. D. Hann, Goodyear Aircraft Corp. *Vice-Chairman*, E. E. Eddey, Goodyear Aircraft Corp. *Secretary*, N. R. Yarosh, Goodyear Aircraft Corp.

Boston—Chairman, H. W. Fuller, Laboratory for Electronics.

Philadelphia—Chairman, L. C. Hobbs. *Vice-Chairman*, L. S. Bensky.

San Francisco—Chairman, L. C. Nofrey, University of California. *Vice-Chairman*, R. W. Melville, Stanford Research Institute. *Secretary*, B. P. Silverman, Friden Calculating Machine Co.

Chapter Meetings

San Francisco—Douglas Englebert, University of California, spoke on "The Gas Discharge Shift Register" in April, and Dr. Noyce, Shockley Division, Beckman Instruments, spoke on "The Transistor as a Switching Device" in May.

Akron—R. A. Kudlich, Bell Telephone Laboratories, spoke on "TRADIC—A Transistor Digital Computer" in April.

Meetings

September 11–12—RETMA Conference on Reliable Electrical Connections, University of Pennsylvania, Irvine Auditorium, Philadelphia, Pa.

September 17–21—ISA Instrument Automation Conference and Exhibit, New York Coliseum, New York, N. Y.

October 1–3—National Electronics Conference and Exhibit, sponsored by AIEE, IRE, Hotel Sherman, Chicago, Ill.

October 9–10—Conference on computer applications, sponsored by the Armour Research Foundation of Illinois Institute of Technology, Chicago, Ill.

December 10–12—IRE-AIEE-ACM Eastern Joint Computer Conference, Hotel New Yorker, New York, N. Y.

January 14–15—Third National Symposium on Reliability and Quality Control in Electronics, sponsored by IRE, RETMA and American Society for Quality Control, Hotel Statler, Washington, D. C.

Army Mathematics Research Center

The Office of Ordnance Research, U. S. Army, has announced the establishment of the Army's Mathematics Research Center at the University of Wisconsin. Dr. R. E. Langer of the Department of Mathematics, University of Wisconsin, has been appointed director of the Research Center. At the present time the Center's offices are located within the Mathematics Department of the University of Wisconsin. Ultimately the Center will be housed in a new building to be constructed by the University. The significance attached to the Center by Army research policy makers is indicated by their stated intention of funding it, when at full strength, at an annual cost of approximately $800,000.

The general objective of the Army in establishing the Center is to provide a nucleus of highly qualified mathematicians responsive to the Army, who will carry on investigations slanted toward general problems having Army relevance, and who can be called upon for advice on problems which may be outside the specific capabilities of Army facilities.

Special Analog-Digital Issue Of Transactions

It was announced in the March, 1956 issue that this issue of the Transactions on Electronic Computers was to be devoted to papers where analog and digital techniques were used together. No papers in this specific area were received in time for publication. Therefore, this issue is not devoted to the special field originally proposed. Several good papers, including some in the area of checking analog computations have been received or are promised. Appropriate papers from this group will be published in future issues.

Stanley B. Disson
News Editor
Burroughs Res. Center
Paoli, Pa

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NOTICE—Readers who are mounting their reviews, and hence wish alternate pages to be left blank are requested to write to the editor, R. E. Meagher, University of Illinois, Urbana, Ill., indicating their wish that this arrangement be continued. Unless a number of readers request this, the blank pages will be discontinued.—*The Editor*

Reviews of Current Literature

It is the intention of this section to review articles that have been published since January 1, 1953, and to publish eventually reviews of all books pertaining to the computer field. Authors can be of considerable assistance in this review process by sending two reprints of their articles to H. D. Huskey, Department of Electrical Engineering, University of California, Berkeley, California. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.—*Harry D. Huskey*

GENERAL

56-97

Man Viewed as a Machine—John G. Kemeny. (*Scientific American*, vol. 192, pp. 58–67; April, 1955.) A comparison of man and computer, in terms of speed, power, and memory. The human memory has a capacity corresponding to between 10^6 and 10^8 binary bits of machine storage. This leads to the conclusion that machines have not yet imitated the human brain's method of storing and recovering information. A discussion of the question, "Can a machine think?", is presented with a description of the Turing machine. The Turing machine is used in the discussion to develop a universal machine which can imitate if it is supplied with a description of a task and of the special machine which solves the task. A very interesting discussion of a reproducing machine is presented. The reproductive concept is defined and the procedure of reproduction is demonstrated. Many analogies between machines and the human organism are described.

J. A. Fingerett

56-98

Computers and Engineering Education—Paul E. Stanley. (*Computers and Automation*, vol. 5, pp. 10–12; February, 1956.) The introduction of an analog computer into the curriculum can—in addition to teaching the use of the computer—provide a means for emphasizing the similarity between systems in different fields of engineering. A computer with the necessary capability could be constructed by an institution for a reasonable cost.

Gordon Morrison

56-99

What is a Computer?—Neil MacDonald. (*Computers and Automation*, vol. 5, pp. 12–14, 46; January, 1956.) There is a tendency, in tutorial papers of this type, to make things so simple that a ten-year-old can understand what is said. Unfortunately this article falls in this category. As a result, it contains so little information that even the most uninitiated reader would gain little knowledge about what a computer really is from reading it. (See 54-211 of December, 1954.)

Gordon Morrison

681.142:413.164 56-100

Glossary of Terms relating to Automatic Digital Computers, B. S. 2641:1955 (Book Notice)—Publishers: British Standards Institution, London, 1955. (*B.S.I. Information Sheet*, p. 2; November, 1955.)

Courtesy of PROC. IRE and *Wireless Engineer*

56-101

Glossary of Terms in the Field of Computers and Automation—(*Computers and Automation*, vol. 5, pp. 15–31; January, 1956.) This is a somewhat more extensive glossary than most of those published in the field. Generally speaking, the definitions seem adequate and compare with those found elsewhere.

Gordon Morrison

56-102

The Physics of Magnetic Materials—R. M. Bozorth. (*Elect. Engrg.*, vol. 75, pp. 134–140; February, 1956.) The author touches briefly on a wide variety of fundamental physical characteristics of magnetic materials. He describes the properties of various types of magnetic materials, and describes the basic phenomena responsible for these properties. The origin of the magnetic moment of several magnetic substances is described in terms of the atomic structure of these substances. A brief description is given of the differences between paramagnetism, ferromagnetism, antiferromagnetism, and ferrimagnetism. Basic properties of various ferrites are discussed, including high frequency phenomena. A discussion of domain structure is given, showing its importance in accounting for the change of magnetism with field. This is followed by a discussion of iron-silicon alloys (used mostly in transformers, generators, motors, etc.) and iron-nickel alloys (used mostly in the communications field).

Harry T. Larson

56-103

Reliability of Electrolytic Capacitors in Computers—M. Van Buskirk. (*Proc. Eastern Computer Conf., Joint IRE-AIEE-ACM, December 8-10, 1953, Washington, D. C.*, pp. 105–109; 1954.) In this article the author states that when electrolytic capacitors are used in applications falling within their limitations no more trouble should be experienced with them than with other electrical components used in computers. Various life test results are described and indicate satisfactory capacitor performance after several years of operation. The problem of electrolytic capacitor storage is discussed. After a long period of shelf storage and before use a capacitor should have low voltage applied and gradually increased until rated voltage is reached. Special derating of operating and surge voltages from standard is recommended. A table which shows "computer ratings" for some typical capacitors is given.

Norman F. Loretz

56-104

Automatic Manufacture of Electronic Equipment—Lawrence P. Lessing. (*Scientific American*, vol. 193, pp. 29–33; August, 1955.) A description is given of the pilot plant, Project Tinkertoy, designed by the National Bureau of Standards. Circuit elements are manufactured with mechanized stages of production and are assembled in modules. Resistors and capacitors are made flat and assembled on wafers with notched sides. The wafers are assembled into modules with riser wires laid into the notches on the sides. The resistors are made by spraying a carbon mixture on an asbestos tape and coating with a plastic film. The resistance tape is later cut into half-inch lengths and applied under pressure between printed electrodes on the wafers. Inductor coils are printed on tiny cylinders. Assembled modules are tested automatically and dipped in a protective plastic coating. The production system is neither completely integrated nor automatic.

J. A. Fingerett

621.374.32 56-105

A Logarithmic Voltage Quantizer—E. M. Glaser and H. Blassbalg. (*Tele-Tech and Electronic Ind.*, vol. 14, pp. 73–75, 128; October, 1955.) Details are given of an analog-to-digital converter which provides an output pulse whose duration is proportional to the logarithm of the input voltage, the output pulse duration being determined by counting the number of fixed-frequency pulses occurring in the same interval. Range of input voltage is 3.3–100 v, with a threshold input pulse length of 0.5 μs.

Courtesy of PROC. IRE and *Wireless-Engineer*

56-106

Detection of Coherent and Non-Coherent Signals—R. F. Drenick, S. Gartenhouse, P. Nesbeda. (*1955 IRE Convention Record*, Pt. 4, pp. 114–118.) The problems of the detection of a signal of unknown frequency in noise, including the case of the received signal being shifted by the Doppler effect, is treated by a statistical theory associated with the name of A. Wald. The presence of an unknown parameter, the signal frequency, makes it a problem of testing a composite hypothesis. Wald's statistical decision function theory leads to decision-making rules (among others) which are optimum in the sense that the greatest mean loss that can possibly accrue to the decision-maker is as small as possible, *i.e.*, a minimax procedure. Two cases met in radar receivers are considered. 1) coherent signal, in which the phase of the signal is known and consistent from sweep to sweep, 2) non-

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coherent signal, in which the phase of the signal from one sweep to the next is assumed to be perfectly random. The optimum (minimax) procedure for establishing the presence of the signal in the two cases is derived.

Eldred C. Nelson

56-107

Analysis of Linear Systems With Randomly Varying Inputs and Parameters—A. Rosenbloom, J. Heilfron, and D. L. Trautman. (*1955 IRE Convention Record*, Pt. 4, pp. 106–113.) This paper surveys certain techniques developed by the authors and others for analyzing the properties of output response of a system subject to randomly varying input signal and parameters. The main approach used in these techniques is the evaluation of the multivariate characteristic function of the output response. From the characteristic function thus evaluated, the multivariate probability distribution function of the output can be obtained by inverse Fourier transform of the characteristic function. The statistical properties of the output can thus be specified. The first part of the paper discussed the case of a fixed linear system subject to input which is either a square Gaussian process or one component of a multidimensional Markoff process. Examples shown are for a first order system but may be generalized to handle higher order systems. The second part concerns systems of randomly varying parameters. In this case, for a first order system, it is possible to determine the characteristic function as certain indefinite time integral of the randomly varying parameter which can be solved by straightforward method or technique described in the first part of the paper. Extension to higher order systems are also briefly mentioned.

Y. C. Ho

56-108

Coding for Noisy Channels—Peter Elias. (*1955 IRE Convention Record*, Pt. 4, pp. 37–46.) This high quality research paper investigates the rate at which the probability of error in signaling over the symmetric binary channel can be made to approach zero by increase in the length of binary code words. Let R be the rate of a discrete source whose messages are encoded into blocks of N binary digits. These binary digits are transmitted over a symmetric binary channel of capacity C. Let $P(N, C, R)$ be the probability of error in the decoded letters when the best possible encoding and decoding schemes are used. The quantity $\alpha(C, R) = \lim_{N\to\infty} -(1/N) \log P(N, C, R)$ is computed explicitly for certain ranges of C and R. For other ranges, inequalities are given for α. Similar results are obtained for restricted classes of codes. In particular, Shannon's ideal rates can be obtained for check symbol and parity check codes and the error decreases exponentially for large N for these codes. All results given are asymptotic for large N. Immediate applications to computer work are not evident.

David Slepian

ANALOG COMPONENT RESEARCH

56-109

Survey of Analog Multiplication Schemes—C. M. Edwards. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 27–35; January, 1954.) This article reviews analog multiplying devices in general use at the time of publication. The survey begins with dynamometer-type and crossed-fields cathode-ray-tube multipliers, an ac similar-triangle-type multiplier, logarithmic and quarter-square multipliers. A number of devices employing feedback to stabilize multiplier gain characteristics are reviewed next, *viz.* servomultipliers, the RCA step multiplier, strain gauge- and vibration-multipliers, AM-fm multipliers, and a frequency-sharing modulation-type multiplier. A brief discussion of pulsed-attenuator or time-division multipliers concludes the survey, which is documented by 24 references to the literature. The article is illustrated by a number of block diagrams and by performance specifications of some typical multipliers. This survey article does not dwell on detailed design problems or on comparisons of the different multiplying devices from a system point of view. It is interesting to note that the material collected by Mr. Edwards in 1953 is still reasonably up to date at the present time. Except for recent improvements in multivariable diode function generators capable of generating the function $f(x, y) = xy$ directly, the only new analog multipliers known to the reviewer are 1) heat-transfer multipliers,[1] which are useful mainly in control-system applications requiring relatively low accuracy, and 2) the Philbrick amplitude-selection multiplier.[2] On the other hand, the performance characteristics of some analog computing devices have been improved very appreciably during the last two years; this is particularly true of time-division multipliers.[2]

G. A. Korn

56-110

A Sub-Audio Time Delay Circuit—C. D. Morrill. (*IRE Trans.*, vol. EC-3, pp. 45–49; June, 1954.) This paper describes a sixth-order electronic differential analyzer circuit for producing a fixed time delay T for input frequencies out to $2/T$ cycles per second. The circuit is synthesized by first computing the transfer function for a fourth order Padé approximation to the ideal time-delay transfer function e^{-sT}. Since this approximation exhibits a slight deviation from the ideal linear phase shift with frequency, a second order transfer function possessing an opposite angular deviation from linear phase shift is added in cascade. The result is a transfer function of unit magnitude with a phase shift within 2 per cent of the ideal linear characteristic out to a frequency-delay product of 12 radians. The electronic differential analyzer circuit for representing the over-all transfer function is given, and an example recording of a delayed signal is presented. The technique employs 10 operational amplifiers and should work for delays up to 60 seconds and more.

R. M. Howe

56-111

Application of a Magnetic Amplifier to a High Performance Instrument Servo—Paul R. Johannessen. (*1955 IRE Convention Record*, Pt. 4, pp. 15–22.) A thorough presentation is made of the advantages of utilizing a magnetic amplifier as the power stage in a high-performance 2-phase motor servomechanism, in particular a two-speed synchro data repeater. In addition to small settling time after slew and high velocity constant and gain cross-over frequency, desired properties were negligible drift and low noise level. The latter characteristic is obtained because the magnetic amplifier is an average-proportional amplifier rather than an instantaneous amplifier. The magnetic amplifier is likewise insensitive to quadrature signals because the integral of such signals over the control half-cycle is zero. An interesting feature is the summing of an ac error signal and a dc tachometer signal. Adequate circuit diagrams and response curves are provided.

Louis B. Wadel

ANALOG EQUIPMENT

681.142:621.37 56-112

The Isograph—an Electronic Root Finder—A. K. Choudhury. (*Indian J. Phys.*, vol. 29, pp. 468–473; October, 1955.) The instrument described is designed on the principle of harmonic synthesis, short-circuited and open-circuited delay lines fed from a matched frequency-sweep generator being used to produce the sine and cosine terms respectively. By controlling the amount of frequency sweep, any desired interval of the argument can be expanded and the accuracy of the measurement thus increased.

Courtesy of Proc. IRE and *Wireless Engineer*

UTILIZATION OF ANALOG EQUIPMENT

56-113

Industrial Uses of Analog Computers—R. L. Hovious, C. D. Morrill, and N. P. Tomlinson. (*The Computer Handbook*, edited by Milton H. Aronson, The Instruments Publishing Co., Pittsburgh, Pa., pp. 10–17; 1955.) This paper describes the basic operation of electronic analog computers. The linear functions of integration, differentiation, addition, and transport delay are discussed as are the nonlinear functions of multiplication and back-lash. Block diagrams and system equations for a process control system, a position servomechanism and a dc motor serve as examples to illustrate application of the computer to practical problems. The paper contains a listing of typical applications and a statement of advantages of the type computer described. It concludes with mention of the widespread availability of computer facilities which on a rental basis permit individual acquisition of experience and evaluation without a large investment. As the authors point out, nothing basically new is contained in the paper. It provides however, a useful introduction to the electronic analog computer and its application. It does so at a practical level and in readable style.

Don Lebell

56-114

Analysis of Combined Sampled and Continuous-Data Systems on an Electronic Analog Computer—L. B. Wadel. (*1955 IRE Convention Record*, Pt. 4, pp. 3–7.) This in-

[1] P. H. Savet, "Analog computing by heat transfer," *Tele-Tech.*, February, 1954.

[2] George A. Philbrick Researches, Data Sheet for Type Mu Multiplying Component. G. A. Korn and T. M. Korn, "Electronic Analog Computers," 2nd edition, McGraw-Hill Book Co., Inc., New York, N. Y.; 1956.

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teresting scheme represents control-system-dynamics by a conventional computer setup on an existing dc analog computer. Each sampling-holding device is represented by a dc integrator specially connected so as to assume the *reset* condition when the computer is in the *hold* condition, and the *hold* condition when the computer is in the *compute* condition.[1] A special timing circuit periodically places the computer in the *hold* condition for a time interval sufficient to "reset" each storage integrator to the last-computed value of a variable to be sampled; the storage integrators "hold" these sample values and introduce them into the computer setup during the subsequent *compute* period. The next sample is then taken at a suitably chosen time, and the cycle repeats. This stepwise computing scheme represents sampling and data storage with a minimum of special equipment, but it is not directly applicable to real-time simulation. Mr. Wadel's use of dc integrators as storage devices acquires added significance when it is viewed in the context of other automatic or semi-automatic programming techniques applicable to analog computers. Such techniques include preset automatic programming,[2] digital readout, and automatic checking circuits;[3] with the addition of storage integrators and of relays or electronic comparators implementing logical decisions one obtains sequential automatic programming,[4] automatic scale-factor changes,[5] and simulation of complex random processes such as duels and traffic problems. Such schemes combine the high-speed all-parallel arithmetic of analog computers with digital-computer logic. The development of a few special computing elements to replace the jury-rigged relay trees used in early combination setups of this type might open an entire new field of interesting applications.

G. A. Korn

DIGITAL COMPONENT RESEARCH

56-115

Computer Memories—Louis N. Ridenour. (*Scientific American*, vol. 192, pp. 92–100; June, 1955.) The application of a memory system in a computer is described by a comparison with physical information devices used by men. Machine memory requirements are defined as being in three classes: high speed, intermediate-speed, and large-capacity storage. For the high speed memory system, vacuum-tube toggle, mercury delay tank, electrostatic memory, and magnetic core storage techniques are described. Limitations of each type are discussed. Magnetic drum storage and magnetic core arrays are described as useful for the larger, intermediate-speed storage. The large-capacity storage techniques described include punched card, magnetic tape, and photoscopic storage. The limitations of punched cards and magnetic tape techniques are given. Little work has been done on photoscopic storage for computers. The technique of photoscopic disk memory is illustrated to describe the operation.

J. A. Fingerett

539.152.2:538.569.4 56-116

Spin-Echo Memory Device—S. Fernbach and W. G. Proctor. (*J. Appl. Phys.*, vol. 26, pp. 170–181; February, 1955.) "A proton-rich sample placed in a strong inhomogeneous magnetic field of mean strength H_0 was subjected to a pattern of relatively weak radio-frequency pulses at the Larmor frequency of the protons in the field H_0. The pattern was then recalled by applying a strong rf pulse at a later time as in the spin-echo technique. It is shown both mathematically and experimentally that such a series of pulses, varying in amplitude can be 'memorized' by the spin system of protons for times as long as one second and then repeated, preserving both shape and relative amplitude." Spin echoes are discussed by Hahn in *Phys. Rev.*, vol. 80, pp. 580–594; November 15, 1950. (See 56-117.)

Courtesy of Proc. IRE and *Wireless Engineer*

538.569.4:539.152.2 56-117

Spin Echo Serial Storage Memory—A. G. Anderson, R. L. Garwin, E. L. Hahn, J. W. Horton, G. L. Tucker, and R. M. Walker. (*J. Appl. Phys.*, vol. 26, pp. 1324–1338; November, 1955.) Methods are discussed for storing information in the form of pulses in a nuclear-magnetic-resonance system, by use of the free-induction spin-echo technique (see 56-116). The storage capacity in liquids is expressed in terms of the thermal noise of the detecting apparatus, the self-diffusion of the molecules, and the relaxation times. Undesired echoes arising from the interaction of input pulses are eliminated by frequency- and magnetic-field-modulation techniques. Glycerin and solutions of paramagnetic ions in water provide storage times of 10–50 ms, with a storage capacity of the order of 1000 echoes. Larger capacities expected from liquids with long relaxation times are not realized owing to self-diffusion.

Courtesy of Proc. IRE and *Wireless Engineer*

621.385.832:681.142 56-118

Digital Memory in Barrier-Grid Storage Tubes—M. E. Hines, M. Chruney, and J. A. McCarthy. (*Bell Syst. Tech. J.*, vol. 34, pp. 1241–1264; November, 1955.) A description is given of the operation of a cr tube in which the same beam is used for writing and reading signals in the form of charges on a dielectric plate held between the barrier grid and a backplate; storage capacity and probability of error due to amplifier noise are particularly discussed. Experimental tubes have been produced with a capacity of 16,000 information bits, with reading and writing times of about 1 μs.

Courtesy of Proc. IRE and *Wireless Engineer*

681.142:538.221 56-119

Magnetic Core Circuits for Digital Data-Processing Systems—D. Loev, W. Miehle, J. Paivinen, and J. Wylen. (Proc. IRE, vol. 44, pp. 154–162; February, 1956.) Circuits for interconnecting toroidal cores used to perform various functions in digital computers are discussed. A single-diode loop permits unconditional transfer of information from one or more transmitting cores to one or more receiving cores. A split-winding loop permits conditional transfer and hence logical operations. An inhibit loop is also described. The operation of shift registers, cycle distributors, counters, etc., is explained.

Courtesy of Proc. IRE and *Wireless Engineer*

56-120

Vacuum and Vibration Speed Assembly of Core Memory Planes—E. A. Guditz and L. B. Smith. (*Electronics*, vol. 29, pp. 214–228; February, 1956.) New techniques used in assembly of core memory planes are described. With the aid of vibration and vacuum, memory cores are made to fall in place in a specially designed plastic form. During wiring a partial vacuum holds the cores in place. A long hypodermic needle is used to thread wires through the 50-mil inside diameter of cores. Completed "mats" of cores are then placed in permanent etched wiring frames. After wiring in frames the cores are immobilized by pouring a cement solution over the mat. The plastic form was designed to accommodate 4096 memory cores. The authors claim a 5 to 1 reduction of assembly time over earlier methods which required 1 to 2 weeks of labor.

Norman F. Loretz

537.227:546.431.824-31 56-121

Ferroelectric Hysteresis in Barium Titanate Single Crystals—H. H. Wieder. (*J. Appl. Phys.*, vol. 26, pp. 1479–1482; December, 1955.) An experimental and theoretical investigation has been made of the hysteresis loop of crystals with antiparallel domains only. Measurements were made over the temperature range $-100°$ to $+100°$C. Coercivity and losses decrease sharply as the crystal passes through the phase transitions from tetragonal to orthorhombic at $-10°$C and from orthorhombic to trigonal at $-90°$C but the loop retains rectangularity. It may be possible by controlling the crystal growth to shift the orthorhombic phase to room temperature.

Courtesy of Proc. IRE and *Wireless Engineer*

621.375.43:681.142 56-122

Transistor Amplifiers for Use in a Digital Computer—Q. W. Simkins and J. H. Vogelsong. (Proc. IRE, vol. 44, pp. 43–55; January, 1956.) Pulse-regenerative amplifiers for a 3 mc synchronous binary computer are based on use of external feedback, so that a negative-resistance transistor characteristic is not required. By using semigated feedback, allowance can be made for the slow recovery of Ge diodes incorporated in the circuit.

Courtesy of Proc. IRE and *Wireless Engineer*

56-123

The Typotron, A Novel Character Display Storage Tube—H. M. Smith. (*1955 IRE Convention Record*, Pt. 4, pp. 129–134.) This paper describes the principles of operation, performance characteristics, and construction of the Hughes Typotron tube. This tube is a special-purpose cathode-ray tube that combines the Convair Charactron's ability to display letters and numbers

[1] G. A. Korn and T. M. Korn, "Electronic Analog Computers," 2nd edition, The McGraw-Hill Book Co., Inc., New York, N. Y.; 1956.
[2] G. R. Hansen, "The Time-Sequency Controller for Automatic Operation of the Electronic Analyzer." Memo 2-81, Jet Propulsion Lab., Calif. Inst. of Tech. Pasadena, Calif.; March 2, 1953.
[3] Korn and Korn, *op. cit.*, and R. D. McCoy and B. D. Loveman, "Problem checker checks computer, too," *Control Engr.*, July, 1955.
[4] L. B. Wadel, "Automatic Iteration on an Electronic Analog Computer," Western Electronics Show and Convention, Los Angeles, Calif.; 1954.
[5] "Automatic Scale-Changing Attachment for GEDA Computers," Report GER 5839, Goodyear Aircraft Corp., Akron, Ohio; June 4, 1955.

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—*The Editor*

n printed-page format with the Hughes Memotron's ability to retain a display indefinitely. The Typotron will be useful as temporary visual-storage device for alphaumerical information. The paper is well-rganized, well-written, and concise. It prorides the reader with a clear and complete icture of the essentials of the Typotron.

Stanley Rogers

56-124

Basic Circuits Used in Digital Automaion—Martin L. Klein, Frank K. Williams, nd Harry C. Morgan. (*Instruments and Automation*, vol. 29, pp. 271–279; February, 956.)This article, one of a series on digital ontrol methods, begins with a description f vacuum tube operation and goes on to how how the vacuum tube is employed in igital control circuits. Principles of operaion are given for ac and dc amplifiers; athode followers; multivibrators, including he flip-flop; blocking oscillators; gating circuits; and several types of wave-shaping and lamping circuits. The use of neon diodes or memory and logical applications is also overed.

Vernon C. Kamm

56-125

Quarterly Report No. 9, Second Series—. R. Bowman, A. Milch, et al. (*Quart. Rept. Computer Components Fellowship Mellon Inst.*, 56 pp. + ix; October 1, 1955 to December 31, 1955.) The report is divided nto two parts. Part I deals, in three sections, vith high temperature printed circuitry. The structure, composition, and behavior f resistors, capacitors, and conducting eads materialized on glass and ceramic ubstrates are discussed from the point of iew of vacuum evaporation and silk creening as two possible modes of formaion. Part II is concerned with electrouminescence. A generalized voltage-brightess relationship is proposed, containing hree arbitrary parameters. There is a ather detailed report on the effects of article size on electroluminescence and hermoluminescence. This work was done n a 1½ pound sample of a General Electric hosphor that had been separated by sedimentation in alcohol into four fractions anging from 2 to 15 microns average diameter. Also noted is a slight shift in the osition of the observed thermoluminescent low peak maxima as a result of quenching y visible light.

A. Milch

DIGITAL SYSTEM RESEARCH

56-126

Coded Decimal Number Systems for Digital Computers—Garland S. White. PROC. IRE, vol. 41, pp. 1450–1452; October, 1953.) Various ways of encoding decimal digits with exactly four binary elements are discussed, with special emphasis on those for which integral weights are assigned to the digit positions. The number of types of such encoding systems is given as 25, and among these the ones in which digit-by-digit binary complementation produces nines complementation is found to be 4. These 14 are rejected as requiring addition circuits which are too complicated. One f the 225 codes is selected as being a coding ystem for which the circuits required for addition, complementation, counting, etc. are all quite simple, and this system is proposed for use in computers to increase economy and reliability.

E. F. Moore

DIGITAL EQUIPMENT

56-127

Simplified Printing Telegraph Switching and Integrated Data Processing—J. B. Booth and R. H. Klich. (*Elec. Engrg.*, vol. 75, pp. 332–335; April, 1956.) This article describes a new teletype typing unit which will be of some interest to designers of data processing systems containing long distance communication links. This unit, designated Teletype Model 28 typing unit, performs some of the switching and remote control functions performed by auxiliary equipment in existing teletype systems. These functions are performed in a "stunt-box" associated with each typing unit. At any given time, either the stunt box or the printing unit is active. Which of these is active is determined by the receipt of a specific character or sequence of characters. In the nonprint condition, the same code combination that resulted in the printing of two different characters (one in lower and one in upper case, determined by the two code combinations used to shift or unshift the platen) may be used to perform two additional functions, either electrical or mechanical, using the stunt box mechanism. The stunt box is described briefly, and selective calling of Model 28 sets is described, including a description of two installations now operating. The use of this equipment in an integrated data processing is indicated in an example order-handling system.

Harry T. Larson

56-128

The Electrographic Recording Technique—H. Epstein. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 116–118; 1955.)

The Electrographic Recording Technique—H. Epstein and F. Innes. (*1955 IRE Convention Record*, Pt. 4, pp. 135–138.) These identical papers present a list of criteria for evaluating printing techniques and an outline of a technique of electrostatic printing. A list of fifteen criteria is presented and it is stated that the most universal technique, consistent with the criteria, is an electrostatic one. The advantages reported are: economy, very high speed capabilities, low power dissipation, relative silence, no moving parts except the paper, no messy wet or damp processes, and permanent recording. The technique involves using seven stylii to deposit characters in the form of a 7×5 matrix of electrically charged spots on moving thermoplastic coated paper. The paper passes a powdered ink which adheres to the charged spots, and heat is used for fixing. A 7×5 core matrix is shown for decoding from character selection lines to impulses for the recordlng stylii. A picture of a laboratory model is shown.

M. M. Astrahan

56-129

Automatic Translation of Printed Code to Impulses Acceptable to Computing Equipment—J. T. Davidson and R. L. Fortune. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 29–33; 1955.) The authors describe a particular system developed by the Standard Register Company for printing and automatically reading data from standard business forms through use of a binary code. This system, called *Stanomatic*, uses special ink in an arrangement of dots 1/16 inch in diameter with ⅛ inch center to center spacing, forming a 5-bit code. The code uses a 1-2-4-7 weighting plus an even parity check. The equipment, using standard pin-fed business forms, can read 500 forms per minute. Each form contains 30 columns of 5-bit coding, *i.e.*, 30 digits per document. Additional groups of 30 digits may be added if desired. Encoding is performed with printing presses, or may be done as a by-product of keyboard operations, using special encoders attached to typewriters or bookkeeping machines. One of the special encoders includes means for printing from an embossed plate on a credit card. Encoded data need not be in the same order as typed data, since the encoding devices provide some format control. The article is concerned entirely with a description of the device. No figures are given concerning reject or error rates.

J. D. Noe

56-130

Ferrite-Core Memory is Fast and Reliable—M. A. Alexander, M. Rosenberg and R. Stuart-Williams. (*Electronics*, vol. 29, pp. 158–161; February, 1956.) The theory and operation of the ferrite-core memory designed for use with the Rand Corporation Johnniac computer is described. This memory has a capacity of 4096 words, each word consisting of 40 binary digits. A parallel mode of operation is used. The time for a read and regenerate cycle or a write cycle is 14½ microseconds (exclusive of addressing time). A 4096 core matrix is constructed in the form of a 128 by 32 rectangle. To select a particular core for interrogation first current is supplied to one row of 128 cores. Then a current pulse is applied to one column of 32 cores from a magnetic core switch. Interrogation in this manner reduces to some degree the undesired noise from unselected cores. Figures in the article present theory and operation of the memory and electronic circuits. The memory is ten feet long, 39 inches wide, and 19 inches high. It contains 1207 tubes, 288 germanium diodes, 5120 switch cores, and 168,960 storage cores. The authors state that the mean error free operating time exceeds 35 hours.

Norman F. Loretz

56-131

Industrial Uses of Special-Purpose Computers—A. H. Kuhnel. (*The Computer Handbook*, edited by Milton H. Aronson, The Instruments Publishing Co., Pittsburgh, Pa., pp. 4–9; 1955.) Following a brief discussion of the fundamental characteristics of analog and digital computers, the author describes three examples of special-purpose computers. One controls the selection between two thicknesses of stock in building up a stack of motor laminations to a specified over-all dimension. A second computer controls the speed of work rotation in a turbine-blade milling machine in order to produce uniform effective feed rate. The third device measures digitally and records on magnetic tape the instantaneous positions of a number of rotating shafts

E. C. Johnson

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—*The Editor*

56-132

SEER, a Sequence Extrapolating Robot—D. W. Hagelbarger. (*IRE Trans.*, vol. EC-5, pp. 1–7; March, 1956.) The author of this article introduces a relay machine designed at Bell Telephone Laboratories to play and win a simple guessing game. The object of this game is for the machine to guess the next in a sequence of pluses and minuses "played" by its human opponent. The author states that out of 9795 plays against visitors and employees at Bell Telephone Laboratories the machine has won 5218 times and lost 4577 times. These results cannot be explained on the basis of chance alone. The article presents a series of "learning curves" illustrating the performance of the machine in coming to recognize and predict four simple sequences. The author states that the machine tends to win more than half the time against any simple sequence. The author discusses the usefulness of such a machine, pointing out that by means of a few minor changes the machine would become an "environment-adapting machine"; and furthermore, in extremely complicated situations, a machine that would learn to be efficient might be easier to design than an efficient machine as such. Also included in the article are: a detailed discussion of the strategy used by the machine, an appendix covering circuit logic and operation of the machine, and an appendix discussing strategies for beating the machine.

Jack L. Hursch, Jr.

681.142 56-133

The Program-Controlled Electronic Computer at Munich (PERM)—H. Piloty, R. Piloty, H. O. Leilich, and W. E. Proebster. (*Nachrichtentech. Z.*, vol. 8, pp. 603–609; November, and pp. 650–658; December, 1955.) Detailed illustrated description of a machine designed for calculations on scientific problems. A binary internal system is combined with a decimal external system. The word length is 50 binary digits. The magnetic-drum store rotates at 250 rps; mean access time is 2 ms and capacity is 8192 words. Teleprinter tape is used for input and output, with photoelectric scanning also for the input. 2400 tubes and 3000 Ge diodes are used; the power consumption is less than 11 kw.

Courtesy of PROC. IRE and *Wireless Engineer*

UTILIZATION OF DIGITAL EQUIPMENT

56-134

The Planning Behind the IBM 702 Installation at Chrysler Corporation—Eugene Lindstrom. (*Computers and Automation*, vol. 5, pp. 13–15, 32; February, 1956.) The 702 installation referred to is applied to five activities within the parts department. These are central inventory control, central invoicing, sales cost determination, central accounts receivable, and sales analysis. A thumbnail sketch of these applications is presented in the article, but very little is said about the planning which led to the operations and which the title implies is the purpose of the article.

Gordon Morrison

56-135

Logic on Electronic Computers: A Practical Method for Reducing Expressions to Conjunctive Normal Form—N. A. Routledge. (*Proc. Camb. Phil. Soc.*, vol. 52, pp. 161–173; April, 1956.) A method of programming a computer to solve the decision problem in the propositional calculus is outlined and proof of its validity is given. The method is based on converting the given expression into the conjunctive normal form but avoids the necessity of storing the whole of the normal form at one time. A method of generating the terms individually is given, based on relating these terms to numbers expressed in binary form. The method has been programmed for the ACE Pilot model which can handle expressions of up to 160 symbols.

S. Gill

56-136

Translation by Machine—William N. Locke. (*Scientific American*, vol. 194, pp. 29–33; January, 1956.)A history of machine translation is presented from its birth in 1946. Some discussion of the economics is made by a comparison of machine costs with those of manual translation. Word by word translation is illustrated by an example and compared with an expert translation. The process of machine translation is described, and the state-of-the-art is discussed for each basic step involved. Many references are made to workers in the field.

J. A. Fingerett

56-137

The Chess Machine: An Example of Dealing with a Complex Task by Adaptation—Allen Newell. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 101–108; 1955.) In this paper the author discusses programming a computer to play chess as an illustration of a complex problem which machines might be able to deal with by "adaptation." Various aspects of the chess playing problem are outlined such as: goals and tactics, level of aspiration, evaluation of positions, choice of important moves for consideration, language to be used by the machine, and possibilities for learning on the part of the machine. These problems are then discussed on a very broad and general level. No attempt is made to go into detail, but rather to present a fund of ideas for further exploration.

Jack L. Hursch, Jr.

56-138

Linear Filtering of Sampled Data—Gene Franklin. (*1955 IRE Convention Record*, Pt. 4, pp. 119–128.) This paper is an application of Weiner's least squares filtering theory to a situation where a time stationary random message plus noise are sampled before being filtered. The correlation functions and power density spectrums of the sampled signals are derived and compared to their continuous signal counterparts. These functions are then used to obtain the optimum linear filter in the least square sense by way of the Weiner-Hopf equation. An example is presented of the design of a linear filter to reconstruct and predict a sampled random function in the absence of noise. An important aspect of the result is that the filter must be realized by a discrete data network such as a linear program on a digital computer in addition to the usual lumped parameter RLC network. There is no discussion of any complexities in the solution which may arise because of mixed rational functions in e^{sT} and s. Nor is there any development into the various conditions which give rise to a discrete filter in addition to the continuous filter.

Maier Margolis

56-139

A General Digital Computer Program for Static Stress Analysis—P. H. Denke and I. V. Boldt. (*Proc. 1955 Western Joint Computer Conference, Los Angeles, Calif.*, pp. 72–78; *1955.*) This paper describes a general digital-computer program, applicable to a large class of aircraft structures without additional programming time, for static stress analysis on an IBM 701 with 2048 word electrostatic storage, four magnetic drums, and four magnetic tape units. Computing times for the various matrix operations are given. Principles are stated by means of which satisfactory computational accuracy can usually be attained.

Thomas H. Southard

56-140

Automatic Computation of Nerve Excitation—K. S. Cole, H. A. Antosiewicz, and P. Rabinowitz. (*Jour. Soc. Industrial and Applied Math.*, vol. 3, pp. 153–172; September, 1955.) This paper describes the numerical integration on SEAC, by the Runge-Kutta method, of a system of four nonlinear ordinary differential equations with initial conditions (equations attributed to Hodgkin and Huxley), which system describes the functioning of a single nerve fiber. Comparisons are made with results previously computed by Hodgkin and Huxley.

Thomas H. Southard

56-141

Application of Data Processors in Production—C. R. DeCarlo. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 61–65; 1955.) This paper reviews briefly some of the applications of the IBM 701 EDPM to certain production control problems at the IBM Endicott Production Division. It starts by listing some of the difficulties which rather uniquely characterize the utilization of data processing equipment in the field of production control, then proceeds to describe how at least some parts of the production control problem have been handled within certain restricted assumptions. Dr. DeCarlo outlines a scheduling application on the 701, using the so-called "synthesis" method. This method utilizes the product of the parts assembly matrix by the production schedule vectors, but also includes the effect of additional vectors representing the "common parts usage." He also described a procedure on the 701, to derive the Predicted Machine Load and Raw Material Forecast for the Endicott plants for 1955. This procedure was presented in more detail but the schedule period was so long (280 days) that one wonders how feasible the program would be (considering the numerous changes which periodically must up-date the main files) for a job-shop operation requiring scheduling over a much shorter period. The author presents some valuable suggestions for further research and refinements in these operations (some of which have evidently already been commenced), and points out such important considerations as the fact that a linear program to establish a schedule with uniform machine loading is not necessarily the schedule with the minimum cost. In addition to the somewhat obvious suggestions for im-

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—*The Editor*

provement in a production scheduling operation, such as better sales and production forecasts and improvement in engineering standard techniques, he recommends: 1) the development of stochastic models (for such chance variables as machine breakdown, operator performance, rejection rates, etc.); 2) the application of combinatorial analysis to the problem (now feasible with high speed computers); 3) the extension of linear programming techniques to "permit the simultaneous estimation of time scheduled activities and cost or profit functions."

Neal J. Dean

56-142

An Optimization Concept for Business Data-Processing Equipment—D. R. Swanson (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 43–48; 1955.) The author describes various techniques for optimizing either the cost or speed of a business data processing system. These techniques involve calculations with various parameters which attempt to characterize the class of jobs which the system is to process and the properties of the tape units and "processors" which comprise the system. The independent variables whose values are sought in the optimization are: 1) the number of processors and 2) the number of tape units. The practical value of the techniques described to a prospective purchaser of a data-processing system may be limited by the following considerations. 1) It is not clear what effect various simplifying assumptions will have on the validity of the result. 2) It appears difficult to estimate the values of certain parameters employed which characterize "average" properties of all the jobs the system is to process. 3) In practical situations the major question is often the selection of one of several different types of processors and one of several types of tape units. The techniques described appear to be difficult to apply in answering such questions. 4) Certain parameters which are known to have a strong influence on the economic effectiveness of a data processing system are omitted from consideration, for example, cost of program preparation. Thus the cost of program preparation for an integrated system having more than 1 processor might be so great as to make the system far from optimal even though the techniques discussed here might indicate quite the reverse.

John W. Bacus

56-143

Data Collection as a By-Product of Normal Business Machine Operation—J. C. Taylor. (*Proc. 1955 Western Joint Computer Conf., Los Angeles, Calif.*, pp. 34–41; 1955.) The author presents a very good description of a "point of sale" development by the National Cash Register Company without evaluating the merits of this particular system. A rather straightforward description of the method used is given. It is not new. The reviewer understands that another company has one or two actual installations of equipment similar to that described in the article. The concept of the system assumes that it is desirable to capture additional information at the point of sale, and there is no quarrel with this. The question is—how much—since to do much of the accounting job one would need more experienced help or more automatic equipment. The many variations that must be considered in dealing with department store customers such as: delivery charges, wrapping charges, separation of state and federal taxes, employee's discounts, etc., poses a large problem for the efficient operation of this type of system.

R. J. Abele

56-144

The Organization of a Program Library for a Digital Computer Center—Werner L. Frank. (*Computers and Automation*, vol. 5, pp. 6–8; March, 1956.) The efficient operation of a computing center depends on the efficient use of its program library. This, in turn, requires systematic organization of the identification code used with the library routines as well as the standardization of their format. In addition, the index should include a description of the routines which is organized so that each routine is described in a standard manner. Finally, the index must be properly circulated to those who make use of the equipment.

Gordon Morrison

56-145

The Function of Automatic Programming for Computers in Business Data Processing—R. E. Rossheim. (*Computers and Automation*, vol. 5, pp. 6–9, 32; February, 1956.) Almost everyone seems to accept the idea that automatic programming can be of considerable assistance in most applications of large computing equipment. In the business field, this assistance can include streamlining training procedures, facilitation of approximation procedures, and speeding program checking and modification. In addition it is expected that, in the future, this technique can be extended to allow the machine to operate directly from the flow chart.

Gordon Morrison

56-146

Automatic Coding Techniques for Business Data Processing, Directions of Development—Charles W. Adams and Bruse Moncreiff. (*Computers and Automation*, vol. 5, pp. 10–11, 35; January, 1956.) This reprint of a personal letter from Moncreiff to Adams is written in a facetious and sarcastic manner which is often used in such communications but which has no place in technical or semitechnical literature. The criticism of current techniques is of the "eggs in the fan" type while the techniques which he proposes (which are mentioned only briefly) seem to be only slightly different fundamentally from those which he criticizes.

Gordon Morrison

56-147

Growth of IBM Electronic Data Processing Operations on the West Coast—Neil MacDonald. (*Computers and Automation*, vol. 5, pp. 10–13; March, 1956.) Computer activity is rapidly expanding on the West Coast; however, the degree of this expansion or even its absolute value is not indicated in this article. A few examples of installations and equipment on order from one manufacturer are given. On the other hand, no data on the number of installations from preceding years or the current year is given. This article, which merely says that a particular manufacturer has a large number of machines installed, or on order, in the West Coast area, would be much better titled "IBM Is Doing a Big Business on the West Coast."

Gordon Morrison

BOOK REVIEWS

56-148

Proc. RETMA Symposium on Automation, University of Pennsylvania, September, 1955; Sponsored by Engr. Dept. of Radio-Electronic-Television Manufacturers Assoc.—(Engineering Publishers GPO, Box 1151, New York, 114 pp.; 1956.) The papers in these proceedings deal chiefly with automation for high volume assembly and low volume production, data processing and utilization, and redesign for automatic production. Some of the specific subjects discussed are automatic production of electronic assemblies, automatic ware-housing, factory automation by digital control, and production of electronic circuits by mechanized wiring. The proceedings also include a panel discussion on the future of automation.

Courtesy of *Electrical Engineering*

56-149

Introduction to Electronic Analog Computers—C. A. A. Wass. (McGraw-Hill Book Co., Inc., New York, 220 pp., 9 p. index + 6 p. appendix × x p., 149 figs.; 1955.) This is a book primarily about real-time electronic analog computers (*i.e.*, "differential analyzers" and "simulators," the distinction being more a point of view than a difference in equipment). Network, repetitive, and ac simulators are touched on only lightly. It is a book for people who use machines of this type and want to understand them rather than for those who design them. Two of the early chapters and one of the late ones are given over to discussions of ways of using analog computers. These discussions center on a series of increasingly complex problems and should be helpful to those who are not already experts. Two features of the book merit special notice. First, the author analyzes major problems in the design of dc operational amplifiers and points out many limitations on amplifier performance. He derives expressions that enable the reader to compute the magnitudes of certain errors made by practical amplifiers. These include errors caused by finite gain, grid current, and equivalent drift voltage, referred to input grid. The consequences of phase shift in the forward open-loop gain are touched lightly. Summing-junction capacitance and the errors it creates are not dealt with. Some readers may be surprised to learn that, percentage-wise, feedback makes one kind of error worse and does nothing to reduce another. For gains less than unity, one may want to use a pot instead of more feedback. Secondly, the book contains descriptions of English analog computers which differ in interesting ways from American computers. Both terminology and symbols are, of course, British, but they offer no problem to the American reader. It is apparent, however, that English practice differs in some respects from the American. The author takes a strong stand in the controversy over "open-shop" vs "post-box" methods of using computers. This reviewer liked the "spiral" organization of the book, its up-to-dateness, and its information on British computers. It is well written and easy to read. Recommended.

Stanley Rogers

Courtesy of Proc. IRE

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